Standards Manager Web Standards List

VITA-VMEbus International Trade Association

Id	Number	Title	Year	Organization	Page
1	42.3	XMC PCI Express Protocol Layer Standard - This standard defines the implementation of PCI Express on VITA 42.0, XMC.	2026	VITA	
2	48.1	This standard defines the mechanical requirements that are needed to insure the mechanical interchangeability of air cooled 3U and 6U Plug-In Modules and define the features required to achieve Two Level Maintenance compatibility.	2026	VITA	
3	48.5	Establishes the design requirements for an air-flow-through cooled plug-in unit with a form factor as close to 6U as possible while retaining the VITA 46 connector layout. Unlike ANSI/VITA 48.1, which uses cooling air impinged directly upon the components	2026	VITA	
4	57.1	FPGA Mezzanine Card (FMC) Standard - This standard defines the mechanical format and signal assignments for an FPGA mezzanine card interface.	2026	VITA	
5	57.4	This standard extends the VITA 57.1 FMC standard by specifying two new connectors that enable additional Gigabit Transceiver interfaces that run at up to 28Gbps. It also describes FMC+ IO modules which support this enhanced version of the FMC electro-mech	2026	VITA	
6	62.2	This standard provides requirements for building a 270 volt/3U or 6U class power supply module that can be used to power a VPX chassis in the VITA 62 family of standards in high altitude applications.	2026	VITA	
7	67.2	Coaxial Interconnect on VPX, 8 Position SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a VITA 46 interface containing multi-position blind mate analog connecto	2026	VITA	
8	78.0	SpaceVPX Systems	2026	VITA	
9	90.0 ERTA	VNX+ Base Standard	2026	VITA	
10	90.1 ERTA	VNX+ Profile Tables	2026	VITA	
11	90.2 ERTA	VNX+ Optical and RF Connector Modules - Type 2	2026	VITA	
12	90.3 ERTA	VNX+ Power Supply and Storage Modules	2026	VITA	
13	90.4	VNX+ Cooling and Mounting Systems	2026	VITA	
14	65.0	OpenVPX System Standard	2025	VITA	
15	65.1	This standard documents variations of Slot, Backplane, and Modules Profiles. As part of the Slot Profile Description, there are also some Connector Modules defined. This document is primarily tables which are referenced by [VITA 65.0]. PDF Version.	2025	VITA	
16	66.3	Optical Interconnect On VPX - Mini-Expanded Beam Variant â__The VITA 66.3 standard defines an MT Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2025	VITA	
17	67.0	Coaxial Interconnect on VPX - Base Standard - The objective of this standard is to establish a structure for implementing blind mate analog coaxial interconnects with VPX backplanes and plug-in modules, and to define a specific family of interconnects and	2025	VITA	
18	67.1	Coaxial Interconnect on VPX, 3U, 4 Position, SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a 3U VITA 46 interface containing multi-position blind mate analog	2025	VITA	
19	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2025	VITA	
20	93.0	QMC - Small Form Factor Mezzanine	2025	VITA	
21	1.5	2eSST - This standard defines a new VME protocol that allows data transfers of up to 320 Mbytes/second. Reaffirmed in 2009. Stabilized in 2014.	2025	VITA	
22	1.7	Increased Current DIN Connector- This standard describes increased current levels, test methods, test data and compliance criteria for 3 row DIN and 5 row DIN connectors when used in VME, VME64 and VME64 Extension P1/J1 and P2/J2 pin out arrangements.	2025	VITA	

23	32	Processor PMC - This standard incorporates a set of extensions to the IEEE 1386.1 PMC (__PCI Mezzanine Card__) standard which creates a new class of CPU based PMC cards referred to in this standard as Processor PMC cards.	2025	VITA	
24	60.0	Alternative Connector for VPX - This standard provides an alternate connector to the one specified in the VITA 46.0 VPX Baseline Standard. Because the 46.0 and the 60.0 connectors are not intermateable, a VITA 60.0 module will not plug into a VITA 46.0.0	2025	VITA	
25	46.4	PCI Express_ on the VPX Fabric Connector - The objective of this standard is the implementation of the PCI Express_ Fabric in the VITA46 environment and to define the mapping of the PCI Express Links on the VPX connector.	2025	VITA	0
26	46.6	Gigabit Ethernet Control Plane on VPX - The objectives of this standard are to assign Gigabit Ethernet Port mappings for the purpose of Control Plane communication onto the VPX connectors for both 3U and 6U form factors and to provide rules and recommenda	2025	VITA	0
27	46.31	Higher Data Rate VPX, Solder Tail	2025	VITA	0
28	47.1	Common Requirements for Environments, Design and Construction, Safety, and Quality for VITA 47 Plug-In Modules Dot Standard.	2025	VITA	0
29	51.1	Reliability Prediction MIL-HDBK-217 Subsidiary Specification	2025	VITA	0
30	51.2	Physics of Failure Reliability Predictions - This specification provides standard processes, instructions and default parameters for using the Physics of Failure (PoF) approach for modeling the reliability of electronic products. It includes a discussion	2025	VITA	0
31	66.0	Optical Interconnect on VPX - Base Standard -- The VITA 66.0 base standard defines physical features of a stand-alone compliant blind mate Optical Interconnect for use in VPX systems.	2025	VITA	0
32	66.2	Optical Interconnect On VPX - ARINC 801 Termini Variant â__The VITA 66.2 standard defines an ARINC 801 Termini Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2025	VITA	0
33	66.4	Optical Interconnect On VPX - Half Width MT Variant	2025	VITA	0
34	68.0	VITA 68.0 is the Base Standard of the VITA 68.x family of standards for signal integrity compliance of VPX systems and components.	2025	VITA	0
35	68.1	VPX Compliance Channel - Fixed Signal Integrity Budget Standard	2025	VITA	0
36	86	High Voltage Input Sealed Connector Power Supply	2025	VITA	0
37	17.3	Serial Front Panel Data Port (sFPDP) Gen 3.0	2025	VITA	
38	40	Service and Status Indicator Standard. This standard defines the colors, behaviors, placement, and labeling of service indicator lamps for boards, field replaceable units, and enclosures.	2025	VITA	
39	47.0	Construction, Safety, and Quality for Plug-In Modules Standard	2025	VITA	
40	47.2	Class 2 Requirements for Environments, Design and Construction, Safety, and Quality for VITA 47 Plug-In Modules Dot Standard	2025	VITA	
41	47.3	Class 3 Requirements for Environments, Design and Construction, Safety, and Quality for VITA 47 Plug-In Modules Dot Standard	2025	VITA	
42	68.3	Reference SI Model Standard for Gen4 and Higher Speeds	2024	VITA	0
43	87.0	High Density (HD) MT Circular Connector - Type 1	2024	VITA	0
44	91.0	Connector for Higher Density VPX Applications	2024	VITA	0
45	42.6	XMC 10 Gigabit Ethernet 4-Lane Protocol Layer Standard - This standard defines a method for supporting 10 Gigabit Ethernet using XAUI switched interconnect protocol on the XMC form factor.	2024	VITA	0
46	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2024	VITA	0
47	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2024	VITA	0
48	42.3	XMC PCI Express Protocol Layer Standard - This standard defines the implementation of PCI Express on VITA 42.0, XMC.	2024	VITA	0
49	46.7	Ethernet on VPX Fabric Connector - The objectives of this standard are to assign backplane Ethernet links to the VPX P1/J1 connector and to provide rules and recommendations for the use of Ethernet over backplane media.	2024	VITA	0
50	46.9	PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard - This VITA 46 (VPX) subsidiary standard defines PMC or XMC mezzanine rear I/O pin mappings to VITA 46.0 plug-in module backplane connectors.	2024	VITA	0

51	46.10	Rear Transition Module for VPX	2024	VITA	0
52	49.2	The ANSI/VITA 49.2 standard, which is part of the VITA Radio Transport (VRT) family of standards, defines a signal/spectrum protocol that expresses spectrum observation, spectrum operations, and capabilities of RF devices. This is done independent of manu	2024	VITA	0
53	51.0	Reliability Prediction - This document provides an electronics failure rate prediction standard, and establishes a Community of Practice. It addresses the limitations of existing prediction practices with a series of subsidiary specifications that contain	2024	VITA	0
54	51.3	Qualification and Environmental Stress Screening in Support of Reliability Predictions - This standard provides rules, permissions, and observations to assure that cost effective Qualification and Environmental Stress Screening support valid reliability p	2024	VITA	0
55	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2023	VITA	0
56	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2023	VITA	0
57	48.7	Mechanical Standard for Electronic Plug-in units using Air Flow-By Cooling Technology	2023	VITA	0
58	62.1	Three Phase High-Voltage Power Supply Front- End in a 3U Plug-In Module Standard	2023	VITA	0
59	65.0	OpenVPX System Standard	2023	VITA	0
60	65.1	This standard documents variations of Slot, Backplane, and Modules Profiles. As part of the Slot Profile Description, there are also some Connector Modules defined. This document is primarily tables which are referenced by [VITA 65.0].	2023	VITA	0
61	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2023	VITA	0
62	42.0 ERTA	XMC	2023	VITA	0
63	17	Front Panel Data Port (FPDP) - This standard defines a point to point data interconnect for use on front panel Eurocard modules.	2022	VITA	
64	23	VME64 Extensions for Physics - This standard defines a series of recommended practices for the use of VMEbus in the physics community.	2022	VITA	
65	26	Myrinet - This standard defines a packet switched interconnect protocol for implementation in a VMEbus environment.	2022	VITA	
66	30.1	2mm Connector Practice for Conduction Cooled Euroboard Systems - This standard defines the dimensions for conduction cooled Euroboards when used with 2mm connectors.	2022	VITA	
67	42.1	XMC Switched Mezzanine Card: Parallel RapidIOâ__ 8/16 LP-LVDS Protocol Layer Standard - This standard defines the implementation of Parallel RIO on VITA 42.0, XMC.	2022	VITA	0
68	30	2mm Connector Practice for Euroboard Systems - This standards provides the dimensions for Euroboard systems that use 2mm connectors.	2022	VITA	
69	3	Board Level Live Insertion - This standard defines several methodologies for using VMEbus modules in a live insertion framework.	2022	VITA	
70	4.1	IP I/O Mapping to VME64x - This standard defines the pin assignments from IP Modules to the VME64x P0 and P2 connectors.	2022	VITA	
71	4	IP Module - This standard defines the requirements for a business card sized mezzanine module printed circuit board.	2022	VITA	
72	5.1	RACEway Interlink - This standard defines a high speed circuit switched point to point interconnect for use between VMEbus modules via the P2 connector.	2022	VITA	
73	6.1	SCSA Extensions - This standard provides feature extensions to the ANSI/VITA 6 standard.	2022	VITA	
74	6	SCSA - This standard defines an isochronous backplane bus for telephony applications on the VMEbus P2 connector.	2022	VITA	
75	12	M-Module - This standard defines a mezzanine module specification for small sized printed circuit boards.	2022	VITA	
76	17.1	Serial Front Panel Data Port (sFPDP) - This standard defines â__Serial FPDPâ__, a high-speed low-latency serial communications protocol for use in high-speed data transfer applications, typically using a fiber optic link.	2022	VITA	
77	41.6	VXS 1X Gbit Ethernet - This standard describes a method for implementing Ethernet as a control channel on ANSI/VITA 41.0, VXS.	2022	VITA	0
78	66.5 ERTA	Optical Interconnect on VPX - Hybrid Variants	2022	VITA	0
79	46.11	System Management on VPX	2022	VITA	293

80	48.0	Mechanical Specification for Microcomputers Using Ruggedized Enhanced Design Implementation (REDI)	2022	VITA	20
81	48.2	This Standard defines the mechanical requirements that are needed to ensure the mechanical interchangeability of conduction cooled 3U and 6U Plug-In Modules and defines the features required to achieve Two Level Maintenance compatibility.	2022	VITA	60
82	48.4	This standard establishes the mechanical design interface control, outline and mounting requirements for a liquid-flow-through cooled Plug-In Module to ensure the mechanical intermateability of 6U VPX liquid-flow-through cooled Plug-In Module within assoc	2022	VITA	59
83	48.8	Mechanical Standard for Electronic VPX Plug-in Modules Using Air Flow Through Cooling	2022	VITA	54
84	61.0	XMC 2.0 - This standard, based upon VITA 42.0 XMC, defines an open standard for supporting high-speed, switched interconnect protocols on an existing, widely deployed form factor, but utilizing an alternate, ruggedized, high speed mezzanine interconnector	2022	VITA	36
85	62.0	VPX: Modular Power Supply - This standard provides a set of requirements for power supply modules that can be used in VPX systems.	2022	VITA	102
86	66.5	Optical Interconnect on VPX - Hybrid Variants	2022	VITA	84
87	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2022	VITA	77
88	74.0	Compliant System Small Form Factor Module Base Standard	2022	VITA	91
89	78.00	SpaceVPX Systems	2022	VITA	624
90	63.0	Hyperboloid Alternative Connector for VPX	2022	VITA	
91	53.0	Standard for Commercial Technology Market Surveillance â__ This standard describes the types of market surveillance data needed by Department of Defense program managers in order to develop and implement technology refresh plans.	2022	VITA	
92	58.1	Line Replaceable Integrated Electronics Chassis Standard, Liquid Cooled Chassis - The objective of this standard is to identify the particular requirements for a chassis configuration conforming to the ANSI/VITA 58.0 base standard.	2022	VITA	
93	88.0	Switched Mezzanine Card Plus (XMC+) Standard	2021	VITA	44
94	76.0	High Performance Cable Standard - Ruggedized 10 Gbaud Bulkhead Connector for Cu and AOC Cables	2021	VITA	60
95	1.3	VME64x 9U x 400 mm Format - This standard defines a 9U x 400 mm board layout for use within the VMEbus framework	2021	VITA	
96	1.6	Keying for Conduction Cooled VME64x.	2021	VITA	
97	35	Provides pin assignments for PMC P4 connector to VME P0 and P2 connectors.	2021	VITA	
98	49A	Spectrum Survey Interoperability Specification	2021	VITA	
99	42.0	XMC	2021	VITA	83
100	65.0	OpenVPX System Standard	2021	VITA	921
101	65.1	This standard documents variations of Slot, Backplane, and Modules Profiles. As part of the Slot Profile Description, there are also some Connector Modules defined. This document is primarily tables which are referenced by [VITA 65.0].	2021	VITA	80
102	68.2	VPX Standard S-Parameter Definition	2021	VITA	28
103	67.2	Coaxial Interconnect on VPX, 8 Position SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a VITA 46 interface containing multi-position blind mate analog connecto	2020	VITA	28
104	67.2	Coaxial Interconnect on VPX, 8 Position SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a VITA 46 interface containing multi-position blind mate analog connecto	2020	VITA	28
105	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2020	VITA	70
106	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2020	VITA	70
107	62.2	This standard provides requirements for building a 270 volt/3U or 6U class power supply module that can be used to power a VPX chassis in the VITA 62 family of standards in high altitude applications.	2020	VITA	47
108	40	Service and Status Indicator Standard. This standard defines the colors, behaviors, placement, and labeling of service indicator lamps for boards, field replaceable units, and enclosures.	2020	VITA	38
109	46.30	Higher Data Rate VPX	2020	VITA	30

110	48.0	Mechanical Specification for Microcomputers Using Ruggedized Enhanced Design Implementation (REDI)	2020	VITA	16
111	48.1	This standard defines the mechanical requirements that are needed to insure the mechanical interchangeability of air cooled 3U and 6U Plug-In Modules and define the features required to achieve Two Level Maintenance compatibility.	2020	VITA	47
112	48.2	This Standard defines the mechanical requirements that are needed to ensure the mechanical interchangeability of conduction cooled 3U and 6U Plug-In Modules and defines the features required to achieve Two Level Maintenance compatibility.	2020	VITA	54
113	42.3	XMC PCI Express Protocol Layer Standard - This standard defines the implementation of PCI Express on VITA 42.0, XMC.	2020	VITA	40
114	62.2	This standard provides requirements for building a 270 volt/3U or 6U class power supply module that can be used to power a VPX chassis in the VITA 62 family of standards in high altitude applications.	2020	VITA	47
115	40	Service and Status Indicator Standard. This standard defines the colors, behaviors, placement, and labeling of service indicator lamps for boards, field replaceable units, and enclosures.	2020	VITA	38
116	42.3	XMC PCI Express Protocol Layer Standard - This standard defines the implementation of PCI Express on VITA 42.0, XMC.	2020	VITA	40
117	46.30	Higher Data Rate VPX	2020	VITA	30
118	48.0	Mechanical Specification for Microcomputers Using Ruggedized Enhanced Design Implementation (REDI)	2020	VITA	16
119	48.1	This standard defines the mechanical requirements that are needed to insure the mechanical interchangeability of air cooled 3U and 6U Plug-In Modules and define the features required to achieve Two Level Maintenance compatibility.	2020	VITA	47
120	48.2	This Standard defines the mechanical requirements that are needed to ensure the mechanical interchangeability of conduction cooled 3U and 6U Plug-In Modules and defines the features required to achieve Two Level Maintenance compatibility.	2020	VITA	54
121	46.31	Higher Data Rate VPX, Solder Tail	2020	VITA	30
122	46.31	Higher Data Rate VPX, Solder Tail	2020	VITA	31
123	65.0	OpenVPX System Standard	2019	VITA	868
124	47.0	Construction, Safety, and Quality for Plug-In Modules Standard	2019	VITA	26
125	47.1	Common Requirements for Environments, Design and Construction, Safety, and Quality for VITA 47 Plug-In Modules Dot Standard.	2019	VITA	35
126	47.2	Class 2 Requirements for Environments, Design and Construction, Safety, and Quality for VITA 47 Plug-In Modules Dot Standard	2019	VITA	18
127	47.3	Class 3 Requirements for Environments, Design and Construction, Safety, and Quality for VITA 47 Plug-In Modules Dot Standard	2019	VITA	19
128	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2019	VITA	121
129	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2019	VITA	122
130	65.0	OpenVPX System Standard	2019	VITA	868
131	57.1	FPGA Mezzanine Card (FMC) Standard - This standard defines the mechanical format and signal assignments for an FPGA mezzanine card interface.	2019	VITA	80
132	65.1	This standard documents variations of Slot, Backplane, and Modules Profiles. As part of the Slot Profile Description, there are also some Connector Modules defined. This document is primarily tables which are referenced by [VITA 65.0].	2019	VITA	64
133	67.0	Coaxial Interconnect on VPX - Base Standard - The objective of this standard is to establish a structure for implementing blind mate analog coaxial interconnects with VPX backplanes and plug-in modules, and to define a specific family of interconnects and	2019	VITA	26
134	67.1	Coaxial Interconnect on VPX, 3U, 4 Position, SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a 3U VITA 46 interface containing multi-position blind mate analog	2019	VITA	25
135	86	High Voltage Input Sealed Connector Power Supply	2019	VITA	22
136	47.0	Construction, Safety, and Quality for Plug-In Modules Standard	2019	VITA	26

137	47.1	Common Requirements for Environments, Design and Construction, Safety, and Quality for VITA 47 Plug-In Modules Dot Standard.	2019	VITA	35
138	47.2	Class 2 Requirements for Environments, Design and Construction, Safety, and Quality for VITA 47 Plug-In Modules Dot Standard	2019	VITA	18
139	47.3	Class 3 Requirements for Environments, Design and Construction, Safety, and Quality for VITA 47 Plug-In Modules Dot Standard	2019	VITA	19
140	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2019	VITA	122
141	65.1	This standard documents variations of Slot, Backplane, and Modules Profiles. As part of the Slot Profile Description, there are also some Connector Modules defined. This document is primarily tables which are referenced by [VITA 65.0].	2019	VITA	13
142	57.1	FPGA Mezzanine Card (FMC) Standard - This standard defines the mechanical format and signal assignments for an FPGA mezzanine card interface.	2019	VITA	81
143	67.0	Coaxial Interconnect on VPX - Base Standard - The objective of this standard is to establish a structure for implementing blind mate analog coaxial interconnects with VPX backplanes and plug-in modules, and to define a specific family of interconnects and	2019	VITA	26
144	67.1	Coaxial Interconnect on VPX, 3U, 4 Position, SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a 3U VITA 46 interface containing multi-position blind mate analog	2019	VITA	27
145	86	High Voltage Input Sealed Connector Power Supply	2019	VITA	22
146	66.2	Optical Interconnect On VPX - ARINC 801 Termini Variant â__The VITA 66.2 standard defines an ARINC 801 Termini Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2018	VITA	15
147	66.3	Optical Interconnect On VPX - Mini-Expanded Beam Variant â__The VITA 66.3 standard defines an MT Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2018	VITA	16
148	57.4	This standard extends the VITA 57.1 FMC standard by specifying two new connectors that enable additional Gigabit Transceiver interfaces that run at up to 28Gbps. It also describes FMC+ IO modules which support this enhanced version of the FMC electro-mech	2018	VITA	67
149	51.0	Reliability Prediction - This document provides an electronics failure rate prediction standard, and establishes a Community of Practice. It addresses the limitations of existing prediction practices with a series of subsidiary specifications that contain	2018	VITA	28
150	51.1	Reliability Prediction MIL-HDBK-217 Subsidiary Specification	2018	VITA	34
151	60.0	Alternative Connector for VPX - This standard provides an alternate connector to the one specified in the VITA 46.0 VPX Baseline Standard. Because the 46.0 and the 60.0 connectors are not intermateable, a VITA 60.0 module will not plug into a VITA 46.0.0	2018	VITA	45
152	46.1	Rear Transition Module for VPX - This standard defines a rear transition module (RTM) for VPX applications.	2018	VITA	31
153	46.3	Serial RapidIO on VPX Fabric Connector - This standard assigns Serial RapidIO ports to the VPX P1/J1 connector.	2018	VITA	47
154	46.4	PCI Express on the VPX Fabric Connector - The objective of this standard is the implementation of the PCI Express Fabric in the VITA46 environment and to define the mapping of the PCI Express Links on the VPX connector.	2018	VITA	21
155	46.6	Gigabit Ethernet Control Plane on VPX - The objectives of this standard are to assign Gigabit Ethernet Port mappings for the purpose of Control Plane communication onto the VPX connectors for both 3U and 6U form factors and to provide rules and recommenda	2018	VITA	32
156	46.7	Ethernet on VPX Fabric Connector - The objectives of this standard are to assign backplane Ethernet links to the VPX P1/J1 connector and to provide rules and recommendations for the use of Ethernet over backplane media.	2018	VITA	27
157	46.9	PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard - This VITA 46 (VPX) subsidiary standard defines PMC or XMC mezzanine rear I/O pin mappings to VITA 46.0 plug-in module backplane connectors.	2018	VITA	92
158	41.0	VXS VMEbus Switched Serial Standard - This standard defines a method for using switched serial fabrics within the VMEbus framework.	2018	VITA	58
159	41.1	VXS 4X InfiniBandâ__ Protocol Layer Standard - This standard describes a method for using the InfiniBand protocol on ANSI/VITA 41.0, VXS.	2018	VITA	24

160	41.2	VXS 4X Serial RapidIOâ__ Protocol Layer Standard - This standard describes a method for implementing Serial Rapid I/O on ANSI/VITA 41.0, VXS.	2018	VITA	25
161	42.1	XMC Switched Mezzanine Card: Parallel RapidIOâ__ 8/16 LP-LVDS Protocol Layer Standard - This standard defines the implementation of Parallel RIO on VITA 42.0, XMC.	2018	VITA	30
162	42.2	XMC Serial RapidIO Protocol Layer Standard - This standard defines the implementation of Serial RIO on VITA 42.0, XMC.	2018	VITA	15
163	48.4	This standard establishes the mechanical design interface control, outline and mounting requirements for a liquid-flow-through cooled Plug-In Module to ensure the mechanical intermateability of 6U VPX liquid-flow-through cooled Plug-In Module within assoc	2018	VITA	53
164	17.3	Serial Front Panel Data Port (sFPDP) Gen 3.0	2018	VITA	54
165	20	CCPMC - Conduction Cooled PMC - This standard defines the mechanical requirements for compliance with conduction cooled PMC modules.	2018	VITA	19
166	66.2	Optical Interconnect On VPX - ARINC 801 Termini Variant The VITA 66.2 standard defines an ARINC 801 Termini Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2018	VITA	15
167	66.3	Optical Interconnect On VPX - Mini-Expanded Beam Variant The VITA 66.3 standard defines an MT Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2018	VITA	16
168	57.4 ERTA	This standard extends the VITA 57.1 FMC standard by specifying two new connectors that enable additional Gigabit Transceiver interfaces that run at up to 28Gbps. It also describes FMC+ IO modules which support this enhanced version of the FMC electro-mech	2018	VITA	73
169	57.4	This standard extends the VITA 57.1 FMC standard by specifying two new connectors that enable additional Gigabit Transceiver interfaces that run at up to 28Gbps. It also describes FMC+ IO modules which support this enhanced version of the FMC electro-mech	2018	VITA	67
170	42.1	XMC Switched Mezzanine Card: Parallel RapidIO 8/16 LP-LVDS Protocol Layer Standard - This standard defines the implementation of Parallel RIO on VITA 42.0, XMC.	2018	VITA	30
171	42.2	XMC Serial RapidIO Protocol Layer Standard - This standard defines the implementation of Serial RIO on VITA 42.0, XMC.	2018	VITA	15
172	46.1	Rear Transition Module for VPX - This standard defines a rear transition module (RTM) for VPX applications.	2018	VITA	33
173	46.3	Serial RapidIO on VPX Fabric Connector - This standard assigns Serial RapidIO ports to the VPX P1/J1 connector.	2018	VITA	47
174	46.4	PCI Expressì_ on the VPX Fabric Connector - The objective of this standard is the implementation of the PCI Expressì_ Fabric in the VITA46 environment and to define the mapping of the PCI Expressì_ Links on the VPX connector.	2018	VITA	21
175	46.6	Gigabit Ethernet Control Plane on VPX - The objectives of this standard are to assign Gigabit Ethernet Port mappings for the purpose of Control Plane communication onto the VPX connectors for both 3U and 6U form factors and to provide rules and recommenda	2018	VITA	32
176	46.7	Ethernet on VPX Fabric Connector - The objectives of this standard are to assign backplane Ethernet links to the VPX P1/J1 connector and to provide rules and recommendations for the use of Ethernet over backplane media.	2018	VITA	27
177	46.9	PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard - This VITA 46 (VPX) subsidiary standard defines PMC or XMC mezzanine rear I/O pin mappings to VITA 46.0 plug-in module backplane connectors.	2018	VITA	92
178	48.4	This standard establishes the mechanical design interface control, outline and mounting requirements for a liquid-flow-through cooled Plug-In Module to ensure the mechanical intermateability of 6U VPX liquid-flow-through cooled Plug-In Module within assoc	2018	VITA	53
179	51.0	Reliability Prediction - This document provides an electronics failure rate prediction standard, and establishes a Community of Practice. It addresses the limitations of existing prediction practices with a series of subsidiary specifications that contain	2018	VITA	28
180	51.1	Reliability Prediction MIL-HDBK-217 Subsidiary Specification	2018	VITA	34
181	41.0	VXS VMEbus Switched Serial Standard - This standard defines a method for using switched serial fabrics within the VMEbus framework.	2018	VITA	60
182	41.1	VXS 4X InfiniBand Protocol Layer Standard - This standard describes a method for using the InfiniBand protocol on ANSI/VITA 41.0, VXS.	2018	VITA	26

183	41.2	VXS 4X Serial RapidIO Protocol Layer Standard - This standard describes a method for implementing Serial Rapid I/O on ANSI/VITA 41.0, VXS.	2018	VITA	25
184	17.3	Serial Front Panel Data Port (sFPDP) Gen 3.0	2018	VITA	54
185	20	CCPMC - Conduction Cooled PMC - This standard defines the mechanical requirements for compliance with conduction cooled PMC modules.	2018	VITA	19
186	48.8	Mechanical Standard for Electronic VPX Plug-in Modules Using Air Flow Through Cooling	2017	VITA	50
187	49.02	VITA Radio Transport (VRT) Standard for Electromagnetic Spectrum: Signals and Applications	2017	VITA	361
188	49.2	The ANSI/VITA 49.2 standard, which is part of the VITA Radio Transport (VRT) family of standards, defines a signal/spectrum protocol that expresses spectrum observation, spectrum operations, and capabilities of RF devices. This is done independent of manu	2017	VITA	359
189	48.5	Establishes the design requirements for an air-flow-through cooled plug-in unit with a form factor as close to 6U as possible while retaining the VITA 46 connector layout. Unlike ANSI/VITA 48.1, which uses cooling air impinged directly upon the components	2017	VITA	33
190	53.0	Standard for Commercial Technology Market Surveillance This standard describes the types of market surveillance data needed by Department of Defense program managers in order to develop and implement technology refresh plans.	2017	VITA	24
191	65.1	This standard documents variations of Slot, Backplane, and Modules Profiles. As part of the Slot Profile Description, there are also some Connector Modules defined. This document is primarily tables which are referenced by [VITA 65.0]. PDF Version.	2017	VITA	58
192	65.0	OpenVPX System Standard	2017	VITA	769
193	68.1	VPX Compliance Channel - Fixed Signal Integrity Budget Standard	2017	VITA	46
194	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2017	VITA	41
195	68.0	VITA 68.0 is the Base Standard of the VITA 68.x family of standards for signal integrity compliance of VPX systems and components.	2017	VITA	25
196	68.1 ERTA	VPX Compliance Channel - Fixed Signal Integrity Budget Standard	2017	VITA	49
197	74.0	Compliant System Small Form Factor Module Base Standard	2017	VITA	92
198	48.5	Establishes the design requirements for an air-flow-through cooled plug-in unit with a form factor as close to 6U as possible while retaining the VITA 46 connector layout. Unlike ANSI/VITA 48.1, which uses cooling air impinged directly upon the components	2017	VITA	32
199	49.2	The ANSI/VITA 49.2 standard, which is part of the VITA Radio Transport (VRT) family of standards, defines a signal/spectrum protocol that expresses spectrum observation, spectrum operations, and capabilities of RF devices. This is done independent of manu	2017	VITA	359
200	48.8	Mechanical Standard for Electronic VPX Plug-in Modules Using Air Flow Through Cooling	2017	VITA	50
201	53.0	Standard for Commercial Technology Market Surveillance â__ This standard describes the types of market surveillance data needed by Department of Defense program managers in order to develop and implement technology refresh plans.	2017	VITA	24
202	68.0	VITA 68.0 is the Base Standard of the VITA 68.x family of standards for signal integrity compliance of VPX systems and components.	2017	VITA	24
203	68.1 ERTA	VPX Compliance Channel - Fixed Signal Integrity Budget Standard	2017	VITA	51
204	74.0	Compliant System Small Form Factor Module Base Standard	2017	VITA	92
205	66.4	Optical Interconnect On VPX - Half Width MT Variant	2016	VITA	19
206	66.0	Optical Interconnect on VPX - Base Standard -- The VITA 66.0 base standard defines physical features of a stand-alone compliant blind mate Optical Interconnect for use in VPX systems.	2016	VITA	22
207	62.0	VPX: Modular Power Supply - This standard provides a set of requirements for power supply modules that can be used in VPX systems.	2016	VITA	97
208	51.2	Physics of Failure Reliability Predictions - This specification provides standard processes, instructions and default parameters for using the Physics of Failure (PoF) approach for modeling the reliability of electronic products. It includes a discussion	2016	VITA	46

209	51.3	Qualification and Environmental Stress Screening in Support of Reliability Predictions - This standard provides rules, permissions, and observations to assure that cost effective Qualification and Environmental Stress Screening support valid reliability p	2016	VITA	21
210	41.6	VXS 1X Gbit Ethernet - This standard describes a method for implementing Ethernet as a control channel on ANSI/VITA 41.0, VXS.	2016	VITA	36
211	42.0	XMC	2016	VITA	44
212	68.1	VPX Compliance Channel - Fixed Signal Integrity Budget Standard	2016	VITA	47
213	68.0	VITA 68.0 is the Base Standard of the VITA 68.x family of standards for signal integrity compliance of VPX systems and components.	2016	VITA	26
214	76.0	High Performance Cable Standard - Ruggedized 10 Gbaud Bulkhead Connector for Cu and AOC Cables	2016	VITA	61
215	78.00 ERTA	SpaceVPX Systems	2016	VITA	410
216	66.0	Optical Interconnect on VPX - Base Standard -- The VITA 66.0 base standard defines physical features of a stand-alone compliant blind mate Optical Interconnect for use in VPX systems.	2016	VITA	22
217	66.4	Optical Interconnect On VPX - Half Width MT Variant	2016	VITA	19
218	67.1 ERTA	Coaxial Interconnect on VPX, 3U, 4 Position, SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a 3U VITA 46 interface containing multi-position blind mate analog	2016	VITA	24
219	62	Modular Power Supply Standard	2016	VITA	97
220	60.0	Alternative Connector for VPX - This standard provides an alternate connector to the one specified in the VITA 46.0 VPX Baseline Standard. Because the 46.0 and the 60.0 connectors are not intermateable, a VITA 60.0 module will not plug into a VITA 46.0.0	2016	VITA	45
221	51.2	Physics of Failure Reliability Predictions - This specification provides standard processes, instructions and default parameters for using the Physics of Failure (PoF) approach for modeling the reliability of electronic products. It includes a discussion	2016	VITA	46
222	51.3	Qualification and Environmental Stress Screening in Support of Reliability Predictions - This standard provides rules, permissions, and observations to assure that cost effective Qualification and Environmental Stress Screening support valid reliability p	2016	VITA	21
223	41.6	VXS 1X Gbit Ethernet - This standard describes a method for implementing Ethernet as a control channel on ANSI/VITA 41.0, VXS.	2016	VITA	36
224	42.0	XMC	2016	VITA	44
225	42.6	XMC 10 Gigabit Ethernet 4-Lane Protocol Layer Standard - This standard defines a method for supporting 10 Gigabit Ethernet using XAUI switched interconnect protocol on the XMC form factor.	2015	VITA	17
226	49A	Spectrum Survey Interoperability Specification	2015	VITA	44
227	49.0	The VITA Radio Transport (VRT) standard defines a transport-layer protocol designed to promote interoperability between RF (radio frequency) receivers and signal processing equipment in a wide range of applications.	2015	VITA	184
228	46.10	Rear Transition Module for VPX	2015	VITA	38
229	46.11	System Management on VPX	2015	VITA	228
230	17.1	Serial Front Panel Data Port (sFPDP) - This standard defines Serial FPDP, a high-speed low-latency serial communications protocol for use in high-speed data transfer applications, typically using a fiber optic link.	2015	VITA	42
231	63.0	Hyperboloid Alternative Connector for VPX	2015	VITA	43
232	49.1	This standard specifies an optional encapsulation protocol for VITA-49.0 (VRT) packets.	2015	VITA	18
233	78.00	SpaceVPX Systems	2015	VITA	404
234	17.1	Serial Front Panel Data Port (sFPDP) - This standard defines â__Serial FPDPâ__, a high-speed low-latency serial communications protocol for use in high-speed data transfer applications, typically using a fiber optic link.	2015	VITA	42
235	46.10	Rear Transition Module for VPX	2015	VITA	38
236	46.11	System Management on VPX	2015	VITA	228

237	49A	Spectrum Survey Interoperability Specification	2015	VITA	44
238	49.0	The VITA Radio Transport (VRT) standard defines a transport-layer protocol designed to promote interoperability between RF (radio frequency) receivers and signal processing equipment in a wide range of applications.	2015	VITA	184
239	49.1	This standard specifies an optional encapsulation protocol for VITA-49.0 (VRT) packets.	2015	VITA	18
240	42.6	XMC 10 Gigabit Ethernet 4-Lane Protocol Layer Standard - This standard defines a method for supporting 10 Gigabit Ethernet using XAUI switched interconnect protocol on the XMC form factor.	2015	VITA	17
241	63.0	Hyperboloid Alternative Connector for VPX	2015	VITA	43
242	78.00	SpaceVPX Systems	2015	VITA	410
243	61.0	XMC 2.0 - This standard, based upon VITA 42.0 XMC, defines an open standard for supporting high-speed, switched interconnect protocols on an existing, widely deployed form factor, but utilizing an alternate, ruggedized, high speed mezzanine interconnector	2014	VITA	25
244	58.0	This standard provides common design and performance requirements for a family of integrated electronic chassis incorporating updated industry standard high speed electronic assemblies and designed for rugged environments.	2014	VITA	27
245	39	PCI-X for PMC and Processor PMC - This standard integrates the PCI-X capability from PCI to PMC based products, including standard PMCs as well as Processor PMCs.	2014	VITA	11
246	48.7	Mechanical Standard for Electronic Plug-in units using Air Flow-By Cooling Technology	2014	VITA	37
247	30.1	2mm Connector Practice for Conduction Cooled Euroboard Systems - This standard defines the dimensions for conduction cooled Euroboards when used with 2mm connectors.	2014	VITA	34
248	31.1	Gigabit Ethernet on VME64x Backplanes - This standard defines a pin assignment and interconnection methodology for implementing a 10/100/1000BASE-T Ethernet switched network on a ANSI/VITA 1.1 VME64x backplane.	2014	VITA	17
249	32	Processor PMC - This standard incorporates a set of extensions to the IEEE 1386.1 PMC (PCI Mezzanine Card) standard which creates a new class of CPU based PMC cards referred to in this standard as Processor PMC cards.	2014	VITA	15
250	1.7	Increased Current DIN Connector- This standard describes increased current levels, test methods, test data and compliance criteria for 3 row DIN and 5 row DIN connectors when used in VME, VME64 and VME64 Extension P1/J1 and P2/J2 pin out arrangements.	2014	VITA	11
251	1.5	2eSST - This standard defines a new VME protocol that allows data transfers of up to 320 Mbytes/second	2014	VITA	48
252	61.0	XMC 2.0 - This standard, based upon VITA 42.0 XMC, defines an open standard for supporting high-speed, switched interconnect protocols on an existing, widely deployed form factor, but utilizing an alternate, ruggedized, high speed mezzanine interconnector	2014	VITA	25
253	58.0	This standard provides common design and performance requirements for a family of integrated electronic chassis incorporating updated industry standard high speed electronic assemblies and designed for rugged environments.	2014	VITA	27
254	30.1	2mm Connector Practice for Conduction Cooled Euroboard Systems - This standard defines the dimensions for conduction cooled Euroboards when used with 2mm connectors.	2014	VITA	35
255	31.1	Gigabit Ethernet on VME64x Backplanes - This standard defines a pin assignment and interconnection methodology for implementing a 10/100/1000BASE-T Ethernet switched network on a ANSI/VITA 1.1 VME64x backplane.	2014	VITA	17
256	32	Processor PMC - This standard incorporates a set of extensions to the IEEE 1386.1 PMC (PCI Mezzanine Card) standard which creates a new class of CPU based PMC cards referred to in this standard as Processor PMC cards.	2014	VITA	15
257	39	PCI-X for PMC and Processor PMC - This standard integrates the PCI-X capability from PCI to PMC based products, including standard PMCs as well as Processor PMCs.	2014	VITA	11
258	1.5	2eSST - This standard defines a new VME protocol that allows data transfers of up to 320 Mbytes/second	2014	VITA	48
259	1.7	Increased Current DIN Connector- This standard describes increased current levels, test methods, test data and compliance criteria for 3 row DIN and 5 row DIN connectors when used in VME, VME64 and VME64 Extension P1/J1 and P2/J2 pin out arrangements.	2014	VITA	11
260	48.7	Mechanical Standard for Electronic Plug-in units using Air Flow-By Cooling Technology	2014	VITA	37
261	42.0	XMC	2014	VITA	40
262	42.3	XMC PCI Express Protocol Layer Standard - This standard defines the implementation of PCI Express on VITA 42.0, XMC.	2014	VITA	37

263	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2013	VITA	109
264	46.1	Rear Transition Module for VPX - This standard defines a rear transition module (RTM) for VPX applications.	2013	VITA	33
265	46.9 ERTA	PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard - This VITA 46 (VPX) subsidiary standard defines PMC or XMC mezzanine rear I/O pin mappings to VITA 46.0 plug-in module backplane connectors.	2013	VITA	71
266	46.6	Gigabit Ethernet Control Plane on VPX - The objectives of this standard are to assign Gigabit Ethernet Port mappings for the purpose of Control Plane communication onto the VPX connectors for both 3U and 6U form factors and to provide rules and recommenda	2013	VITA	32
267	46.11	System Management on VPX	2013	VITA	208
268	51.1	Reliability Prediction MIL-HDBK-217 Subsidiary Specification	2013	VITA	34
269	38	Describes a methodology for using IPMI for System Management of VME systems.	2013	VITA	18
270	58.1	Line Replaceable Integrated Electronics Chassis Standard, Liquid Cooled Chassis - The objective of this standard is to identify the particular requirements for a chassis configuration conforming to the ANSI/VITA 58.0 base standard.	2013	VITA	27
271	66.2	Optical Interconnect On VPX - ARINC 801 Termini Variant The VITA 66.2 standard defines an ARINC 801 Termini Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2013	VITA	15
272	73.0	VITA 73.0 Rugged Small Form Factor - This document provides mechanical and electrical guidelines for the standardization of switched serial interconnects in small form-factor applications, with specific concern taken to allow deployment in ruggedized envi	2013	VITA	54
273	74.0	Compliant System Small Form Factor Module Base Standard	2013	VITA	67
274	38	Describes a methodology for using IPMI for System Management of VME systems.	2013	VITA	16
275	58.1	Line Replaceable Integrated Electronics Chassis Standard, Liquid Cooled Chassis - The objective of this standard is to identify the particular requirements for a chassis configuration conforming to the ANSI/VITA 58.0 base standard.	2013	VITA	27
276	73.0	VITA 73.0 Rugged Small Form Factor - This document provides mechanical and electrical guidelines for the standardization of switched serial interconnects in small form-factor applications, with specific concern taken to allow deployment in ruggedized envi	2013	VITA	54
277	75.0	VITA 75 Rugged Small Form Factor - This draft standard for a rugged small form factor describes overall subsystem attributes such as the envelope of the subsystem box and the organization of the dot specifications.	2012	VITA	23
278	75.11	This draft standard provides requirements for front panels, connectors, signal pin assignments, and power for VITA 75 subsystems.	2012	VITA	142
279	75.20	Rugged Small Form Factor ù Cooled via Free Air Convection	2012	VITA	26
280	75.22	This draft standard standardizes mounting and cooling for conduction to a cold plate cooled VITA 75 subsystems.	2012	VITA	20
281	66.1	Optical Interconnect On VPX - MT Variant â__The VITA 66.1 standard defines an MT Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2012	VITA	14
282	10	SKYchannel - This standard was withdrawn as an American National Standard in 2012 and is provided for historical reference only. This standard defines a packet switched cross bar interconnect that runs on the VMEbus P2 connector.	2012	VITA	42
283	75.0	VITA 75 Rugged Small Form Factor - This draft standard for a rugged small form factor describes overall subsystem attributes such as the envelope of the subsystem box and the organization of the dot specifications.	2012	VITA	22
284	75.11	This draft standard provides requirements for front panels, connectors, signal pin assignments, and power for VITA 75 subsystems.	2012	VITA	141
285	75.20	Rugged Small Form Factor ù Cooled via Free Air Convection	2012	VITA	25
286	75.22	This draft standard standardizes mounting and cooling for conduction to a cold plate cooled VITA 75 subsystems.	2012	VITA	19
287	12	M-Module - This standard defines a mezzanine module specification for small sized printed circuit boards.	2012	VITA	60
288	65	The OpenVPX System Specification was created to bring versatile system architectural solutions to the VPX market. Based on the extremely flexible VPX family of standards, the OpenVPX standard uses module mechanical, connectors, thermal, communications pro	2012	VITA	555
289	67.1	Coaxial Interconnect on VPX, 3U, 4 Position, SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a 3U VITA 46 interface containing multi-position blind mate analog	2012	VITA	23

290	67.2	Coaxial Interconnect on VPX, 8 Position SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a VITA 46 interface containing multi-position blind mate analog connecto	2012	VITA	24
291	67.0	Coaxial Interconnect on VPX - Base Standard - The objective of this standard is to establish a structure for implementing blind mate analog coaxial interconnects with VPX backplanes and plug-in modules, and to define a specific family of interconnects and	2012	VITA	25
292	66.3	Optical Interconnect On VPX - Mini-Expanded Beam Variant The VITA 66.3 standard defines an MT Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2012	VITA	16
293	60.0	Alternative Connector for VPX - This standard provides an alternate connector to the one specified in the VITA 46.0 VPX Baseline Standard. Because the 46.0 and the 60.0 connectors are not intermateable, a VITA 60.0 module will not plug into a VITA 46.0.0	2012	VITA	45
294	62.0	VPX: Modular Power Supply - This standard provides a set of requirements for power supply modules that can be used in VPX systems.	2012	VITA	91
295	10	SKYchannel - This standard was withdrawn as an American National Standard in 2012 and is provided for historical reference only. This standard defines a packet switched cross bar interconnect that runs on the VMEbus P2 connector.	2012	VITA	44
296	12	M-Module - This standard defines a mezzanine module specification for small sized printed circuit boards.	2012	VITA	62
297	51.0	Reliability Prediction - This document provides an electronics failure rate prediction standard, and establishes a Community of Practice. It addresses the limitations of existing prediction practices with a series of subsidiary specifications that contain	2012	VITA	28
298	46.3	Serial RapidIO on VPX Fabric Connector - This standard assigns Serial RapidIO ports to the VPX P1/J1 connector.	2012	VITA	47
299	46.4	PCI Express on the VPX Fabric Connector - The objective of this standard is the implementation of the PCI Express Fabric in the VITA46 environment and to define the mapping of the PCI Express Links on the VPX connector.	2012	VITA	21
300	46.7	Ethernet on VPX Fabric Connector - The objectives of this standard are to assign backplane Ethernet links to the VPX P1/J1 connector and to provide rules and recommendations for the use of Ethernet over backplane media.	2012	VITA	27
301	42.2	XMC Serial RapidIO Protocol Layer Standard - This standard defines the implementation of Serial RIO on VITA 42.0, XMC.	2012	VITA	17
302	42.1	XMC Switched Mezzanine Card: Parallel RapidIO 8/16 LP-LVDS Protocol Layer Standard - This standard defines the implementation of Parallel RIO on VITA 42.0, XMC.	2012	VITA	32
303	46.8	InfiniBand on VPX Fabric Connector - The objectives of this draft standard are to assign InfiniBand ports to the VPX connectors and to provide rules and recommendations for the use of the assigned InfiniBand ports.	2011	VITA	52
304	51.2	Physics of Failure Reliability Predictions - This specification provides standard processes, instructions and default parameters for using the Physics of Failure (PoF) approach for modeling the reliability of electronic products. It includes a discussion	2011	VITA	57
305	6	SCSA - This standard defines an isochronous backplane bus for telephony applications on the VMEbus P2 connector.	2011	VITA	55
306	4.1	IP I/O Mapping to VME64x - This standard defines the pin assignments from IP Modules to the VME64x P0 and P2 connectors.	2011	VITA	15
307	4	IP Module - This standard defines the requirements for a business card sized mezzanine module printed circuit board.	2011	VITA	97
308	5.1	RACEway Interlink - This standard defines a high speed circuit switched point to point interconnect for use between VMEbus modules via the P2 connector.	2011	VITA	72
309	6.1	SCSA Extensions - This standard provides feature extensions to the ANSI/VITA 6 standard.	2011	VITA	33
310	1.6	Keying for Conduction Cooled VME64x.	2011	VITA	29
311	1	VME64 Standard - This standard covers the main body of the VMEbus specification. It includes both 32 bit and 64 bit usage.	2011	VITA	305
312	3	Board Level Live Insertion - This standard defines several methodologies for using VMEbus modules in a live insertion framework.	2011	VITA	66
313	1.1	VME64 Extensions - This standard covers extensions to the VME64 specification including the 160 pin connector, geographical addressing, and added power pins.	2011	VITA	100

314	1.3	VME64x 9U x 400 mm Format - This standard defines a 9U x 400 mm board layout for use within the VMEbus framework.	2011	VITA	48
315	35	Provides pin assignments for PMC P4 connector to VME P0 and P2 connectors.	2011	VITA	18
316	30	2mm Connector Practice for Euroboard Systems - This standards provides the dimensions for Euroboard systems that use 2mm connectors.	2011	VITA	37
317	41.2	VXS 4X Serial RapidIO Protocol Layer Standard - This standard describes a method for implementing Serial Rapid I/O on ANSI/VITA 41.0, VXS.	2011	VITA	27
318	20	CCPMC - Conduction Cooled PMC - This standard defines the mechanical requirements for compliance with conduction cooled PMC modules.	2011	VITA	21
319	17	Front Panel Data Port (FPDP) - This standard defines a point to point data interconnect for use on front panel Eurocard modules.	2011	VITA	46
320	23	VME64 Extensions for Physics - This standard defines a series of recommended practices for the use of VMEbus in the physics community.	2011	VITA	123
321	26	Myrinet - This standard defines a packet switched interconnect protocol for implementation in a VMEbus environment.	2011	VITA	52
322	66.0	Optical Interconnect on VPX - Base Standard -- The VITA 66.0 base standard defines physical features of a stand-alone compliant blind mate Optical Interconnect for use in VPX systems.	2011	VITA	19
323	66.1	Optical Interconnect On VPX - MT Variant The VITA 66.1 standard defines an MT Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2011	VITA	14
324	17	Front Panel Data Port (FPDP) - This standard defines a point to point data interconnect for use on front panel Eurocard modules.	2011	VITA	46
325	1.6	Keying for Conduction Cooled VME64x.	2011	VITA	27
326	3	Board Level Live Insertion - This standard defines several methodologies for using VMEbus modules in a live insertion framework.	2011	VITA	64
327	4	IP Module - This standard defines the requirements for a business card sized mezzanine module printed circuit board.	2011	VITA	95
328	4.1	IP I/O Mapping to VME64x - This standard defines the pin assignments from IP Modules to the VME64x P0 and P2 connectors.	2011	VITA	13
329	5.1	RACEway Interlink - This standard defines a high speed circuit switched point to point interconnect for use between VMEbus modules via the P2 connector.	2011	VITA	72
330	6	SCSA - This standard defines an isochronous backplane bus for telephony applications on the VMEbus P2 connector.	2011	VITA	53
331	6.1	SCSA Extensions - This standard provides feature extensions to the ANSI/VITA 6 standard.	2011	VITA	31
332	35	Provides pin assignments for PMC P4 connector to VME P0 and P2 connectors.	2011	VITA	16
333	23	VME64 Extensions for Physics - This standard defines a series of recommended practices for the use of VMEbus in the physics community.	2011	VITA	123
334	26	Myrinet - This standard defines a packet switched interconnect protocol for implementation in a VMEbus environment.	2011	VITA	52
335	30	2mm Connector Practice for Euroboard Systems - This standards provides the dimensions for Euroboard systems that use 2mm connectors.	2011	VITA	35
336	1	VME64 Standard - This standard covers the main body of the VMEbus specification. It includes both 32 bit and 64 bit usage.	2011	VITA	303
337	1.1	VME64 Extensions - This standard covers extensions to the VME64 specification including the 160 pin connector, geographical addressing, and added power pins.	2011	VITA	100
338	1.3	VME64x 9U x 400 mm Format - This standard defines a 9U x 400 mm board layout for use within the VMEbus framework	2011	VITA	48
339	46.8	InfiniBand on VPX Fabric Connector - The objectives of this draft standard are to assign InfiniBand ports to the VPX connectors and to provide rules and recommendations for the use of the assigned InfiniBand ports.	2011	VITA	51
340	65	The OpenVPX System Specification was created to bring versatile system architectural solutions to the VPX market. Based on the extremely flexible VPX family of standards, the OpenVPX standard uses module mechanical, connectors, thermal, communications pro	2010	VITA	555

341	57.1	FPGA Mezzanine Card (FMC) Standard - This standard defines the mechanical format and signal assignments for an FPGA mezzanine card interface.	2010	VITA	82
342	53.0	Standard for Commercial Technology Market Surveillance This standard describes the types of market surveillance data needed by Department of Defense program managers in order to develop and implement technology refresh plans.	2010	VITA	24
343	51.3	Qualification and Environmental Stress Screening in Support of Reliability Predictions - This standard provides rules, permissions, and observations to assure that cost effective Qualification and Environmental Stress Screening support valid reliability p	2010	VITA	21
344	48.0	Mechanical Specification for Microcomputers Using Ruggedized Enhanced Design Implementation (REDI)	2010	VITA	17
345	48.5	Establishes the design requirements for an air-flow-through cooled plug-in unit with a form factor as close to 6U as possible while retaining the VITA 46 connector layout. Unlike ANSI/VITA 48.1, which uses cooling air impinged directly upon the components	2010	VITA	33
346	48.2	This Standard defines the mechanical requirements that are needed to ensure the mechanical interchangeability of conduction cooled 3U and 6U Plug-In Modules and defines the features required to achieve Two Level Maintenance compatibility.	2010	VITA	53
347	48.1	This standard defines the mechanical requirements that are needed to insure the mechanical interchangeability of air cooled 3U and 6U Plug-In Modules and define the features required to achieve Two Level Maintenance compatibility.	2010	VITA	48
348	46.9	PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard - This VITA 46 (VPX) subsidiary standard defines PMC or XMC mezzanine rear I/O pin mappings to VITA 46.0 plug-in module backplane connectors.	2010	VITA	70
349	46.4	PCI Express¦_ on the VPX Fabric Connector - The objective of this standard is the implementation of the PCI Express¦_ Fabric in the VITA46 environment and to define the mapping of the PCI Express¦ Links on the VPX connector.	2010	VITA	17
350	46.10	Rear Transition Module for VPX	2009	VITA	38
351	42.6	XMC 10 Gigabit Ethernet 4-Lane Protocol Layer Standard - This standard defines a method for supporting 10 Gigabit Ethernet using XAUI switched interconnect protocol on the XMC form factor.	2009	VITA	19
352	49.1	This standard specifies an optional encapsulation protocol for VITA-49.0 (VRT) packets.	2009	VITA	17
353	49.1	This standard specifies an optional encapsulation protocol for VITA-49.0 (VRT) packets.	2009	VITA	18
354	49.0	The VITA Radio Transport (VRT) standard defines a transport-layer protocol designed to promote interoperability between RF (radio frequency) receivers and signal processing equipment in a wide range of applications.	2009	VITA	179
355	49.0	The VITA Radio Transport (VRT) standard defines a transport-layer protocol designed to promote interoperability between RF (radio frequency) receivers and signal processing equipment in a wide range of applications.	2009	VITA	184
356	41.6	VXS 1X Gbit Ethernet - This standard describes a method for implementing Ethernet as a control channel on ANSI/VITA 41.0, VXS.	2009	VITA	35
357	41.6	VXS 1X Gigabit Ethernet Control Channel Layer Standard	2009	VITA	32
358	31.1	Gigabit Ethernet on VME64x Backplanes - This standard defines a pin assignment and interconnection methodology for implementing a 10/100/1000BASE-T Ethernet switched network on a ANSI/VITA 1.1 VME64x backplane.	2009	VITA	18
359	17.1	Serial Front Panel Data Port (sFPDP) - This standard defines Serial FPDP, a high-speed low-latency serial communications protocol for use in high-speed data transfer applications, typically using a fiber optic link.	2009	VITA	43
360	58.0	This standard provides common design and performance requirements for a family of integrated electronic chassis incorporating updated industry standard high speed electronic assemblies and designed for rugged environments.	2009	VITA	27
361	57.1	FPGA Mezzanine Card (FMC) Standard - This standard defines the mechanical format and signal assignments for an FPGA mezzanine card interface.	2008	VITA	79
362	30.1	2mm Connector Practice for Conduction Cooled Euroboard Systems - This standard defines the dimensions for conduction cooled Euroboards when used with 2mm connectors.	2008	VITA	37
363	42.0	XMC	2008	VITA	40
364	46.7	Ethernet on VPX Fabric Connector - The objectives of this standard are to assign backplane Ethernet links to the VPX P1/J1 connector and to provide rules and recommendations for the use of Ethernet over backplane media.	2008	VITA	21
365	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2007	VITA	109
366	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2007	VITA	107

367	47	This standard defines environmental, design and construction, safety, and quality requirements for commercial-off-the-shelf (COTS) plug-in units (cards, modules, etc.) intended for mobile applications.	2007	VITA	22
368	41.1	VXS 4X InfiniBand Protocol Layer Standard - This standard describes a method for using the InfiniBand protocol on ANSI/VITA 41.0, VXS.	2006	VITA	26
369	41.0	VXS VMEbus Switched Serial Standard - This standard defines a method for using switched serial fabrics within the VMEbus framework.	2006	VITA	60
370	13	VMEbus Pin Assignment Standard for ISO/IEC 14575 (IEEE Std. 1355-1995 (H.I.C.)) - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only.	2006	VITA	14
371	19.1	BusNet Media Access Control - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines the media access control layer for the BusNet backplane software protocol.	2006	VITA	64
372	19.2	BusNet Link Layer Control - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines the link layer control layer for the Busnet backplane software protocol.	2006	VITA	18
373	25	VISION - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines a software application interface for VMEbus modules.	2006	VITA	135
374	29	PC.MIP - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines the mechanical form factor and the pin assignments for a small form factor mezzanine module based on the PCI bus.	2006	VITA	66
375	40	Service and Status Indicator Standard. This standard defines the colors, behaviors, placement, and labeling of service indicator lamps for boards, field replaceable units, and enclosures.	2003	VITA	40
376	17.1	Serial Front Panel Data Port (sFPDP) - This standard defines Serial FPDP, a high-speed low-latency serial communications protocol for use in high-speed data transfer applications, typically using a fiber optic link.	2003	VITA	42
377	1.3	VME64x 9U x 400 mm Format - This standard defines a 9U x 400 mm board layout for use within the VMEbus framework.	2003	VITA	48
378	1.1	VME64 Extensions - This standard covers extensions to the VME64 specification including the 160 pin connector, geographical addressing, and added power pins.	2003	VITA	100
379	40	Service and Status Indicator Standard. This standard defines the colors, behaviors, placement, and labeling of service indicator lamps for boards, field replaceable units, and enclosures.	2002	VITA	37
380	29	PC.MIP - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines the mechanical form factor and the pin assignments for a small form factor mezzanine module based on the PCI bus.	2001	VITA	68
381	30.2	Separable Power Connectors	2001	VITA	
382	1.5	2eSST - This standard defines a new VME protocol that allows data transfers of up to 320 Mbytes/second. Reaffirmed in 2009. Stabilized in 2014.	1999	VITA	51
383	5.1	RACEway Interlink - This standard defines a high speed circuit switched point to point interconnect for use between VMEbus modules via the P2 connector.	1999	VITA	74
384	1.4	VME64x Live Insertion System Requirements	1998	VITA	29
385	26	Myrinet - This standard defines a packet switched interconnect protocol for implementation in a VMEbus environment.	1998	VITA	54
386	23	VME64 Extensions for Physics - This standard defines a series of recommended practices for the use of VMEbus in the physics community.	1998	VITA	125
387	17	Front Panel Data Port (FPDP) - This standard defines a point to point data interconnect for use on front panel Eurocard modules.	1998	VITA	48
388	19.1	BusNet Media Access Control - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines the media access control layer for the BusNet backplane software protocol.	1998	VITA	66
389	19.2	BusNet Link Layer Control - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines the link layer control layer for the Busnet backplane software protocol.	1998	VITA	20
390	19.0	Summary and Introduction to the BusNet Standard	1997	VITA	19
391	25	VISION - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines a software application interface for VMEbus modules.	1997	VITA	137

392	1.1	VME64 Extensions - This standard covers extensions to the VME64 specification including the 160 pin connector, geographical addressing, and added power pins.	1997	VITA	98
393	1.3	VME64x 9U x 400 mm Format - This standard defines a 9U x 400 mm board layout for use within the VMEbus framework	1997	VITA	50
394	4.1	IP I/O Mapping to VME64x - This standard defines the pin assignments from IP Modules to the VME64x P0 and P2 connectors.	1996	VITA	15
395	6.1	SCSA Extensions - This standard provides feature extensions to the ANSI/VITA 6 standard.	1996	VITA	39
396	12	M-Module - This standard defines a mezzanine module specification for small sized printed circuit boards.	1996	VITA	63
397	10	SKYchannel - This standard was withdrawn as an American National Standard in 2012 and is provided for historical reference only. This standard defines a packet switched cross bar interconnect that runs on the VMEbus P2 connector.	1995	VITA	43
398	13	VMEbus Pin Assignment Standard for ISO/IEC 14575 (IEEE Std. 1355-1995 (H.I.C.)) - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only.	1995	VITA	16
399	4	IP Module - This standard defines the requirements for a business card sized mezzanine module printed circuit board.	1995	VITA	97
400	3	Board Level Live Insertion - This standard defines several methodologies for using VMEbus modules in a live insertion framework.	1995	VITA	66
401	1	VME64 Standard - This standard covers the main body of the VMEbus specification. It includes both 32 bit and 64 bit usage.	1994	VITA	305
402	6	SCSA - This standard defines an isochronous backplane bus for telephony applications on the VMEbus P2 connector.	1994	VITA	55
403	90.7 ERTA	VNX+ Optical and RF Connector Modules - Type 7	1926	VITA	

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