Standards Manager Web Standards List

VITA-VMEbus International Trade Association

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1	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2024	VITA	
2	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2023	VITA	0
3	48.7	Mechanical Standard for Electronic Plug-in units using Air Flow-By Cooling Technology	2023	VITA	0
4	62.1	Three Phase High-Voltage Power Supply Front- End in a 3U Plug-In Module Standard	2023	VITA	0
5	65.0	OpenVPX System Standard	2023	VITA	0
6	65.1	This standard documents variations of Slot, Backplane, and Modules Profiles. As part of the Slot Profile Description, there are also some Connector Modules defined. This document is primarily tables which are referenced by [VITA 65.0].	2023	VITA	0
7	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2023	VITA	
8	46.11	System Management on VPX	2022	VITA	293
9	48.0	Mechanical Specification for Microcomputers Using Ruggedized Enhanced Design Implementation (REDI)	2022	VITA	20
10	48.2	This Standard defines the mechanical requirements that are needed to ensure the mechanical interchangeability of conduction cooled 3U and 6U Plug-In Modules and defines the features required to achieve Two Level Maintenance compatibility.	2022	VITA	60
11	48.4	This standard establishes the mechanical design interface control, outline and mounting requirements for a liquid-flow-through cooled Plug-In Module to ensure the mechanical intermateability of 6U VPX liquid-flow-through cooled Plug-In Module within assoc	2022	VITA	59
12	48.8	Mechanical Standard for Electronic VPX Plug-in Modules Using Air Flow Through Cooling	2022	VITA	54
13	61.0	XMC 2.0 - This standard, based upon VITA 42.0 XMC, defines an open standard for supporting high-speed, switched interconnect protocols on an existing, widely deployed form factor, but utilizing an alternate, ruggedized, high speed mezzanine interconnector	2022	VITA	36
14	62.0	VPX: Modular Power Supply - This standard provides a set of requirements for power supply modules that can be used in VPX systems.	2022	VITA	102
15	66.5	Optical Interconnect on VPX - Hybrid Variants	2022	VITA	84
16	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2022	VITA	77
17	74.0	Compliant System Small Form Factor Module Base Standard	2022	VITA	91
18	78.00	SpaceVPX Systems	2022	VITA	624
19	88.0	Switched Mezzanine Card Plus (XMC+) Standard	2021	VITA	44
20	76.0	High Performance Cable Standard - Ruggedized 10 Gbaud Bulkhead Connector for Cu and AOC Cables	2021	VITA	60
21	42.0	XMC	2021	VITA	83
22	65.0	OpenVPX System Standard	2021	VITA	921
23	65.1	This standard documents variations of Slot, Backplane, and Modules Profiles. As part of the Slot Profile Description, there are also some Connector Modules defined. This document is primarily tables which are referenced by [VITA 65.0].	2021	VITA	80
24	68.2	VPX Standard S-Parameter Definition	2021	VITA	28
25	67.2	Coaxial Interconnect on VPX, 8 Position SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a VITA 46 interface containing multi-position blind mate analog connecto	2020	VITA	28
26	67.2	Coaxial Interconnect on VPX, 8 Position SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a VITA 46 interface containing multi-position blind mate analog connecto	2020	VITA	28
27	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2020	VITA	70

28	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2020	VITA	70
29	62.2	This standard provides requirements for building a 270 volt/3U or 6U class power supply module that can be used to power a VPX chassis in the VITA 62 family of standards in high altitude applications.	2020	VITA	47
30	40	Service and Status Indicator Standard. This standard defines the colors, behaviors, placement, and labeling of service indicator lamps for boards, field replaceable units, and enclosures.	2020	VITA	38
31	46.30	Higher Data Rate VPX	2020	VITA	30
32	48.0	Mechanical Specification for Microcomputers Using Ruggedized Enhanced Design Implementation (REDI)	2020	VITA	16
33	48.1	This standard defines the mechanical requirements that are needed to insure the mechanical interchangeability of air cooled 3U and 6U Plug-In Modules and define the features required to achieve Two Level Maintenance compatibility.	2020	VITA	47
34	48.2	This Standard defines the mechanical requirements that are needed to ensure the mechanical interchangeability of conduction cooled 3U and 6U Plug-In Modules and defines the features required to achieve Two Level Maintenance compatibility.	2020	VITA	54
35	42.3	XMC PCI Express Protocol Layer Standard - This standard defines the implementation of PCI Express on VITA 42.0, XMC.	2020	VITA	40
36	62.2	This standard provides requirements for building a 270 volt/3U or 6U class power supply module that can be used to power a VPX chassis in the VITA 62 family of standards in high altitude applications.	2020	VITA	47
37	40	Service and Status Indicator Standard. This standard defines the colors, behaviors, placement, and labeling of service indicator lamps for boards, field replaceable units, and enclosures.	2020	VITA	38
38	42.3	XMC PCI Express Protocol Layer Standard - This standard defines the implementation of PCI Express on VITA 42.0, XMC.	2020	VITA	40
39	46.30	Higher Data Rate VPX	2020	VITA	30
40	48.0	Mechanical Specification for Microcomputers Using Ruggedized Enhanced Design Implementation (REDI)	2020	VITA	16
41	48.1	This standard defines the mechanical requirements that are needed to insure the mechanical interchangeability of air cooled 3U and 6U Plug-In Modules and define the features required to achieve Two Level Maintenance compatibility.	2020	VITA	47
42	48.2	This Standard defines the mechanical requirements that are needed to ensure the mechanical interchangeability of conduction cooled 3U and 6U Plug-In Modules and defines the features required to achieve Two Level Maintenance compatibility.	2020	VITA	54
43	46.31	Higher Data Rate VPX, Solder Tail	2020	VITA	30
44	46.31	Higher Data Rate VPX, Solder Tail	2020	VITA	31
45	65.0	OpenVPX System Standard	2019	VITA	868
46	47.0	Construction, Safety, and Quality for Plug-In Modules Standard	2019	VITA	26
47	47.1	Common Requirements for Environments, Design and Construction, Safety, and Quality for VITA 47 Plug-In Modules Dot Standard.	2019	VITA	35
48	47.2	Class 2 Requirements for Environments, Design and Construction, Safety, and Quality for VITA 47 Plug-In Modules Dot Standard	2019	VITA	18
49	47.3	Class 3 Requirements for Environments, Design and Construction, Safety, and Quality for VITA 47 Plug-In Modules Dot Standard	2019	VITA	19
50	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2019	VITA	121
51	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2019	VITA	122
52	65.0	OpenVPX System Standard	2019	VITA	868
53	57.1	FPGA Mezzanine Card (FMC) Standard - This standard defines the mechanical format and signal assignments for an FPGA mezzanine card interface.	2019	VITA	80
54	65.1	This standard documents variations of Slot, Backplane, and Modules Profiles. As part of the Slot Profile Description, there are also some Connector Modules defined. This document is primarily tables which are referenced by [VITA 65.0].	2019	VITA	64
55	67.0	Coaxial Interconnect on VPX - Base Standard - The objective of this standard is to establish a structure for implementing blind mate analog coaxial interconnects with VPX backplanes and plug-in modules, and to define a specific family of interconnects and	2019	VITA	26

56	67.1	Coaxial Interconnect on VPX, 3U, 4 Position, SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a 3U VITA 46 interface containing multi-position blind mate analog	2019	VITA	25
57	86	High Voltage Input Sealed Connector Power Supply	2019	VITA	22
58	47.0	Construction, Safety, and Quality for Plug-In Modules Standard	2019	VITA	26
59	47.1	Common Requirements for Environments, Design and Construction, Safety, and Quality for VITA 47 Plug-In Modules Dot Standard.	2019	VITA	35
60	47.2	Class 2 Requirements for Environments, Design and Construction, Safety, and Quality for VITA 47 Plug-In Modules Dot Standard	2019	VITA	18
61	47.3	Class 3 Requirements for Environments, Design and Construction, Safety, and Quality for VITA 47 Plug-In Modules Dot Standard	2019	VITA	19
62	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2019	VITA	122
63	65.1	This standard documents variations of Slot, Backplane, and Modules Profiles. As part of the Slot Profile Description, there are also some Connector Modules defined. This document is primarily tables which are referenced by [VITA 65.0].	2019	VITA	13
64	57.1	FPGA Mezzanine Card (FMC) Standard - This standard defines the mechanical format and signal assignments for an FPGA mezzanine card interface.	2019	VITA	81
65	67.0	Coaxial Interconnect on VPX - Base Standard - The objective of this standard is to establish a structure for implementing blind mate analog coaxial interconnects with VPX backplanes and plug-in modules, and to define a specific family of interconnects and	2019	VITA	26
66	67.1	Coaxial Interconnect on VPX, 3U, 4 Position, SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a 3U VITA 46 interface containing multi-position blind mate analog	2019	VITA	27
67	86	High Voltage Input Sealed Connector Power Supply	2019	VITA	22
68	66.2	Optical Interconnect On VPX - ARINC 801 Termini Variant â__The VITA 66.2 standard defines an ARINC 801 Termini Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2018	VITA	15
69	66.3	Optical Interconnect On VPX - Mini-Expanded Beam Variant â__The VITA 66.3 standard defines an MT Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2018	VITA	16
70	57.4	This standard extends the VITA 57.1 FMC standard by specifying two new connectors that enable additional Gigabit Transceiver interfaces that run at up to 28Gbps. It also describes FMC+ IO modules which support this enhanced version of the FMC electro-mech	2018	VITA	67
71	51.0	Reliability Prediction - This document provides an electronics failure rate prediction standard, and establishes a Community of Practice. It addresses the limitations of existing prediction practices with a series of subsidiary specifications that contain	2018	VITA	28
72	51.1	Reliability Prediction MIL-HDBK-217 Subsidiary Specification	2018	VITA	34
73	60.0	Alternative Connector for VPX - This standard provides an alternate connector to the one specified in the VITA 46.0 VPX Baseline Standard. Because the 46.0 and the 60.0 connectors are not intermateable, a VITA 60.0 module will not plug into a VITA 46.0.0	2018	VITA	45
74	46.1	Rear Transition Module for VPX - This standard defines a rear transition module (RTM) for VPX applications.	2018	VITA	31
75	46.3	Serial RapidIO__on VPX Fabric Connector - This standard assigns Serial RapidIO ports to the VPX P1/J1 connector.	2018	VITA	47
76	46.4	PCI Expressì_ on the VPX Fabric Connector - The objective of this standard is the implementation of the PCI Expressì_ Fabric in the VITA46 environment and to define the mapping of the PCI Expressì Links on the VPX connector.	2018	VITA	21
77	46.6	Gigabit Ethernet Control Plane on VPX - The objectives of this standard are to assign Gigabit Ethernet Port mappings for the purpose of Control Plane communication onto the VPX connectors for both 3U and 6U form factors and to provide rules and recommenda	2018	VITA	32
78	46.7	Ethernet on VPX Fabric Connector - The objectives of this standard are to assign backplane Ethernet links to the VPX P1/J1 connector and to provide rules and recommendations for the use of Ethernet over backplane media.	2018	VITA	27
79	46.9	PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard - This VITA 46 (VPX) subsidiary standard defines PMC or XMC mezzanine rear I/O pin mappings to VITA 46.0 plug-in module backplane connectors.	2018	VITA	92

80	41.0	VXS VMEbus Switched Serial Standard - This standard defines a method for using switched serial fabrics within the VMEbus framework.	2018	VITA	58
81	41.1	VXS 4X InfiniBandâ__ Protocol Layer Standard - This standard describes a method for using the InfiniBand protocol on ANSI/VITA 41.0, VXS.	2018	VITA	24
82	41.2	VXS 4X Serial RapidIOâ__ Protocol Layer Standard - This standard describes a method for implementing Serial Rapid I/O on ANSI/VITA 41.0, VXS.	2018	VITA	25
83	42.1	XMC Switched Mezzanine Card: Parallel RapidIOâ__ 8/16 LP-LVDS Protocol Layer Standard - This standard defines the implementation of Parallel RIO on VITA 42.0, XMC.	2018	VITA	30
84	42.2	XMC Serial RapidIO Protocol Layer Standard - This standard defines the implementation of Serial RIO on VITA 42.0, XMC.	2018	VITA	15
85	48.4	This standard establishes the mechanical design interface control, outline and mounting requirements for a liquid-flow-through cooled Plug-In Module to ensure the mechanical intermateability of 6U VPX liquid-flow-through cooled Plug-In Module within assoc	2018	VITA	53
86	17.3	Serial Front Panel Data Port (sFPDP) Gen 3.0	2018	VITA	54
87	20	CCPMC - Conduction Cooled PMC - This standard defines the mechanical requirements for compliance with conduction cooled PMC modules.	2018	VITA	19
88	66.2	Optical Interconnect On VPX - ARINC 801 Termini Variant The VITA 66.2 standard defines an ARINC 801 Termini Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2018	VITA	15
89	66.3	Optical Interconnect On VPX - Mini-Expanded Beam Variant The VITA 66.3 standard defines an MT Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2018	VITA	16
90	57.4 ERTA	This standard extends the VITA 57.1 FMC standard by specifying two new connectors that enable additional Gigabit Transceiver interfaces that run at up to 28Gbps. It also describes FMC+ IO modules which support this enhanced version of the FMC electro-mech	2018	VITA	73
91	57.4	This standard extends the VITA 57.1 FMC standard by specifying two new connectors that enable additional Gigabit Transceiver interfaces that run at up to 28Gbps. It also describes FMC+ IO modules which support this enhanced version of the FMC electro-mech	2018	VITA	67
92	42.1	XMC Switched Mezzanine Card: Parallel RapidIO 8/16 LP-LVDS Protocol Layer Standard - This standard defines the implementation of Parallel RIO on VITA 42.0, XMC.	2018	VITA	30
93	42.2	XMC Serial RapidIO Protocol Layer Standard - This standard defines the implementation of Serial RIO on VITA 42.0, XMC.	2018	VITA	15
94	46.1	Rear Transition Module for VPX - This standard defines a rear transition module (RTM) for VPX applications.	2018	VITA	33
95	46.3	Serial RapidIO on VPX Fabric Connector - This standard assigns Serial RapidIO ports to the VPX P1/J1 connector.	2018	VITA	47
96	46.4	PCI Expressî_ on the VPX Fabric Connector - The objective of this standard is the implementation of the PCI Expressî_ Fabric in the VITA46 environment and to define the mapping of the PCI Expressî Links on the VPX connector.	2018	VITA	21
97	46.6	Gigabit Ethernet Control Plane on VPX - The objectives of this standard are to assign Gigabit Ethernet Port mappings for the purpose of Control Plane communication onto the VPX connectors for both 3U and 6U form factors and to provide rules and recommenda	2018	VITA	32
98	46.7	Ethernet on VPX Fabric Connector - The objectives of this standard are to assign backplane Ethernet links to the VPX P1/J1 connector and to provide rules and recommendations for the use of Ethernet over backplane media.	2018	VITA	27
99	46.9	PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard - This VITA 46 (VPX) subsidiary standard defines PMC or XMC mezzanine rear I/O pin mappings to VITA 46.0 plug-in module backplane connectors.	2018	VITA	92
100	48.4	This standard establishes the mechanical design interface control, outline and mounting requirements for a liquid-flow-through cooled Plug-In Module to ensure the mechanical intermateability of 6U VPX liquid-flow-through cooled Plug-In Module within assoc	2018	VITA	53
101	51.0	Reliability Prediction - This document provides an electronics failure rate prediction standard, and establishes a Community of Practice. It addresses the limitations of existing prediction practices with a series of subsidiary specifications that contain	2018	VITA	28
102	51.1	Reliability Prediction MIL-HDBK-217 Subsidiary Specification	2018	VITA	34

103	41.0	VXS VMEbus Switched Serial Standard - This standard defines a method for using switched serial fabrics within the VMEbus framework.	2018	VITA	60
104	41.1	VXS 4X InfiniBand Protocol Layer Standard - This standard describes a method for using the InfiniBand protocol on ANSI/VITA 41.0, VXS.	2018	VITA	26
105	41.2	VXS 4X Serial RapidIO Protocol Layer Standard - This standard describes a method for implementing Serial Rapid I/O on ANSI/VITA 41.0, VXS.	2018	VITA	25
106	17.3	Serial Front Panel Data Port (sFPDP) Gen 3.0	2018	VITA	54
107	20	CCPMC - Conduction Cooled PMC - This standard defines the mechanical requirements for compliance with conduction cooled PMC modules.	2018	VITA	19
108	48.8	Mechanical Standard for Electronic VPX Plug-in Modules Using Air Flow Through Cooling	2017	VITA	50
109	49.02	VITA Radio Transport (VRT) Standard for Electromagnetic Spectrum: Signals and Applications	2017	VITA	361
110	49.2	The ANSI/VITA 49.2 standard, which is part of the VITA Radio Transport (VRT) family of standards, defines a signal/spectrum protocol that expresses spectrum observation, spectrum operations, and capabilities of RF devices. This is done independent of manu	2017	VITA	359
111	48.5	Establishes the design requirements for an air-flow-through cooled plug-in unit with a form factor as close to 6U as possible while retaining the VITA 46 connector layout. Unlike ANSI/VITA 48.1, which uses cooling air impinged directly upon the components	2017	VITA	33
112	53.0	Standard for Commercial Technology Market Surveillance This standard describes the types of market surveillance data needed by Department of Defense program managers in order to develop and implement technology refresh plans.	2017	VITA	24
113	65.1	This standard documents variations of Slot, Backplane, and Modules Profiles. As part of the Slot Profile Description, there are also some Connector Modules defined. This document is primarily tables which are referenced by [VITA 65.0]. PDF Version.	2017	VITA	58
114	65.0	OpenVPX System Standard	2017	VITA	769
115	68.1	VPX Compliance Channel - Fixed Signal Integrity Budget Standard	2017	VITA	46
116	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2017	VITA	41
117	68.0	VITA 68.0 is the Base Standard of the VITA 68.x family of standards for signal integrity compliance of VPX systems and components.	2017	VITA	25
118	68.1 ERTA	VPX Compliance Channel - Fixed Signal Integrity Budget Standard	2017	VITA	49
119	74.0	Compliant System Small Form Factor Module Base Standard	2017	VITA	92
120	48.5	Establishes the design requirements for an air-flow-through cooled plug-in unit with a form factor as close to 6U as possible while retaining the VITA 46 connector layout. Unlike ANSI/VITA 48.1, which uses cooling air impinged directly upon the components	2017	VITA	32
121	49.2	The ANSI/VITA 49.2 standard, which is part of the VITA Radio Transport (VRT) family of standards, defines a signal/spectrum protocol that expresses spectrum observation, spectrum operations, and capabilities of RF devices. This is done independent of manu	2017	VITA	359
122	48.8	Mechanical Standard for Electronic VPX Plug-in Modules Using Air Flow Through Cooling	2017	VITA	50
123	53.0	Standard for Commercial Technology Market Surveillance â__ This standard describes the types of market surveillance data needed by Department of Defense program managers in order to develop and implement technology refresh plans.	2017	VITA	24
124	68.0	VITA 68.0 is the Base Standard of the VITA 68.x family of standards for signal integrity compliance of VPX systems and components.	2017	VITA	24
125	68.1 ERTA	VPX Compliance Channel - Fixed Signal Integrity Budget Standard	2017	VITA	51
126	74.0	Compliant System Small Form Factor Module Base Standard	2017	VITA	92
127	66.4	Optical Interconnect On VPX - Half Width MT Variant	2016	VITA	19
128	66.0	Optical Interconnect on VPX - Base Standard -- The VITA 66.0 base standard defines physical features of a stand-alone compliant blind mate Optical Interconnect for use in VPX systems.	2016	VITA	22
129	62.0	VPX: Modular Power Supply - This standard provides a set of requirements for power supply modules that can be used in VPX systems.	2016	VITA	97

130	51.2	Physics of Failure Reliability Predictions - This specification provides standard processes, instructions and default parameters for using the Physics of Failure (PoF) approach for modeling the reliability of electronic products. It includes a discussion	2016	VITA	46
131	51.3	Qualification and Environmental Stress Screening in Support of Reliability Predictions - This standard provides rules, permissions, and observations to assure that cost effective Qualification and Environmental Stress Screening support valid reliability p	2016	VITA	21
132	41.6	VXS 1X Gbit Ethernet - This standard describes a method for implementing Ethernet as a control channel on ANSI/VITA 41.0, VXS.	2016	VITA	36
133	42.0	XMC	2016	VITA	44
134	68.1	VPX Compliance Channel - Fixed Signal Integrity Budget Standard	2016	VITA	47
135	68.0	VITA 68.0 is the Base Standard of the VITA 68.x family of standards for signal integrity compliance of VPX systems and components.	2016	VITA	26
136	76.0	High Performance Cable Standard - Ruggedized 10 Gbaud Bulkhead Connector for Cu and AOC Cables	2016	VITA	61
137	78.00 ERTA	SpaceVPX Systems	2016	VITA	410
138	66.0	Optical Interconnect on VPX - Base Standard -- The VITA 66.0 base standard defines physical features of a stand-alone compliant blind mate Optical Interconnect for use in VPX systems.	2016	VITA	22
139	66.4	Optical Interconnect On VPX - Half Width MT Variant	2016	VITA	19
140	67.1 ERTA	Coaxial Interconnect on VPX, 3U, 4 Position, SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a 3U VITA 46 interface containing multi-position blind mate analog	2016	VITA	24
141	62	Modular Power Supply Standard	2016	VITA	97
142	60.0	Alternative Connector for VPX - This standard provides an alternate connector to the one specified in the VITA 46.0 VPX Baseline Standard. Because the 46.0 and the 60.0 connectors are not intermateable, a VITA 60.0 module will not plug into a VITA 46.0.0	2016	VITA	45
143	51.2	Physics of Failure Reliability Predictions - This specification provides standard processes, instructions and default parameters for using the Physics of Failure (PoF) approach for modeling the reliability of electronic products. It includes a discussion	2016	VITA	46
144	51.3	Qualification and Environmental Stress Screening in Support of Reliability Predictions - This standard provides rules, permissions, and observations to assure that cost effective Qualification and Environmental Stress Screening support valid reliability p	2016	VITA	21
145	41.6	VXS 1X Gbit Ethernet - This standard describes a method for implementing Ethernet as a control channel on ANSI/VITA 41.0, VXS.	2016	VITA	36
146	42.0	XMC	2016	VITA	44
147	42.6	XMC 10 Gigabit Ethernet 4-Lane Protocol Layer Standard - This standard defines a method for supporting 10 Gigabit Ethernet using XAUI switched interconnect protocol on the XMC form factor.	2015	VITA	17
148	49A	Spectrum Survey Interoperability Specification	2015	VITA	44
149	49.0	The VITA Radio Transport (VRT) standard defines a transport-layer protocol designed to promote interoperability between RF (radio frequency) receivers and signal processing equipment in a wide range of applications.	2015	VITA	184
150	46.10	Rear Transition Module for VPX	2015	VITA	38
151	46.11	System Management on VPX	2015	VITA	228
152	17.1	Serial Front Panel Data Port (sFPDP) - This standard defines Serial FPDP, a high-speed low-latency serial communications protocol for use in high-speed data transfer applications, typically using a fiber optic link.	2015	VITA	42
153	63.0	Hyperboloid Alternative Connector for VPX	2015	VITA	43
154	49.1	This standard specifies an optional encapsulation protocol for VITA-49.0 (VRT) packets.	2015	VITA	18
155	78.00	SpaceVPX Systems	2015	VITA	404
156	17.1	Serial Front Panel Data Port (sFPDP) - This standard defines â__Serial FPDPâ__, a high-speed low-latency serial communications protocol for use in high-speed data transfer applications, typically using a fiber optic link.	2015	VITA	42

157	46.10	Rear Transition Module for VPX	2015	VITA	38
158	46.11	System Management on VPX	2015	VITA	228
159	49A	Spectrum Survey Interoperability Specification	2015	VITA	44
160	49.0	The VITA Radio Transport (VRT) standard defines a transport-layer protocol designed to promote interoperability between RF (radio frequency) receivers and signal processing equipment in a wide range of applications.	2015	VITA	184
161	49.1	This standard specifies an optional encapsulation protocol for VITA-49.0 (VRT) packets.	2015	VITA	18
162	42.6	XMC 10 Gigabit Ethernet 4-Lane Protocol Layer Standard - This standard defines a method for supporting 10 Gigabit Ethernet using XAUI switched interconnect protocol on the XMC form factor.	2015	VITA	17
163	63.0	Hyperboloid Alternative Connector for VPX	2015	VITA	43
164	78.00	SpaceVPX Systems	2015	VITA	410
165	61.0	XMC 2.0 - This standard, based upon VITA 42.0 XMC, defines an open standard for supporting high-speed, switched interconnect protocols on an existing, widely deployed form factor, but utilizing an alternate, ruggedized, high speed mezzanine interconnector	2014	VITA	25
166	58.0	This standard provides common design and performance requirements for a family of integrated electronic chassis incorporating updated industry standard high speed electronic assemblies and designed for rugged environments.	2014	VITA	27
167	39	PCI-X for PMC and Processor PMC - This standard integrates the PCI-X capability from PCI to PMC based products, including standard PMCs as well as Processor PMCs.	2014	VITA	11
168	48.7	Mechanical Standard for Electronic Plug-in units using Air Flow-By__ Cooling Technology	2014	VITA	37
169	30.1	2mm Connector Practice for Conduction Cooled Euroboard Systems - This standard defines the dimensions for conduction cooled Euroboards when used with 2mm connectors.	2014	VITA	34
170	31.1	Gigabit Ethernet on VME64x Backplanes - This standard defines a pin assignment and interconnection methodology for implementing a 10/100/1000BASE-T Ethernet switched network on a ANSI/VITA 1.1 VME64x backplane.	2014	VITA	17
171	32	Processor PMC - This standard incorporates a set of extensions to the IEEE 1386.1 PMC (__PCI Mezzanine Card__) standard which creates a new class of CPU based PMC cards referred to in this standard as Processor PMC cards.	2014	VITA	15
172	1.7	Increased Current DIN Connector- This standard describes increased current levels, test methods, test data and compliance criteria for 3 row DIN and 5 row DIN connectors when used in VME, VME64 and VME64 Extension P1/J1 and P2/J2 pin out arrangements.	2014	VITA	11
173	1.5	2eSST - This standard defines a new VME protocol that allows data transfers of up to 320 Mbytes/second	2014	VITA	48
174	61.0	XMC 2.0 - This standard, based upon VITA 42.0 XMC, defines an open standard for supporting high-speed, switched interconnect protocols on an existing, widely deployed form factor, but utilizing an alternate, ruggedized, high speed mezzanine interconnector	2014	VITA	25
175	58.0	This standard provides common design and performance requirements for a family of integrated electronic chassis incorporating updated industry standard high speed electronic assemblies and designed for rugged environments.	2014	VITA	27
176	30.1	2mm Connector Practice for Conduction Cooled Euroboard Systems - This standard defines the dimensions for conduction cooled Euroboards when used with 2mm connectors.	2014	VITA	35
177	31.1	Gigabit Ethernet on VME64x Backplanes - This standard defines a pin assignment and interconnection methodology for implementing a 10/100/1000BASE-T Ethernet switched network on a ANSI/VITA 1.1 VME64x backplane.	2014	VITA	17
178	32	Processor PMC - This standard incorporates a set of extensions to the IEEE 1386.1 PMC (__PCI Mezzanine Card__) standard which creates a new class of CPU based PMC cards referred to in this standard as Processor PMC cards.	2014	VITA	15
179	39	PCI-X for PMC and Processor PMC - This standard integrates the PCI-X capability from PCI to PMC based products, including standard PMCs as well as Processor PMCs.	2014	VITA	11
180	1.5	2eSST - This standard defines a new VME protocol that allows data transfers of up to 320 Mbytes/second	2014	VITA	48
181	1.7	Increased Current DIN Connector- This standard describes increased current levels, test methods, test data and compliance criteria for 3 row DIN and 5 row DIN connectors when used in VME, VME64 and VME64 Extension P1/J1 and P2/J2 pin out arrangements.	2014	VITA	11
182	48.7	Mechanical Standard for Electronic Plug-in units using Air Flow-By__ Cooling Technology	2014	VITA	37
183	42.0	XMC	2014	VITA	40

184	42.3	XMC PCI Express Protocol Layer Standard - This standard defines the implementation of PCI Express on VITA 42.0, XMC.	2014	VITA	37
185	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2013	VITA	109
186	46.1	Rear Transition Module for VPX - This standard defines a rear transition module (RTM) for VPX applications.	2013	VITA	33
187	46.9 ERTA	PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard - This VITA 46 (VPX) subsidiary standard defines PMC or XMC mezzanine rear I/O pin mappings to VITA 46.0 plug-in module backplane connectors.	2013	VITA	71
188	46.6	Gigabit Ethernet Control Plane on VPX - The objectives of this standard are to assign Gigabit Ethernet Port mappings for the purpose of Control Plane communication onto the VPX connectors for both 3U and 6U form factors and to provide rules and recommenda	2013	VITA	32
189	46.11	System Management on VPX	2013	VITA	208
190	51.1	Reliability Prediction MIL-HDBK-217 Subsidiary Specification	2013	VITA	34
191	38	Describes a methodology for using IPMI for System Management of VME systems.	2013	VITA	18
192	58.1	Line Replaceable Integrated Electronics Chassis Standard, Liquid Cooled Chassis - The objective of this standard is to identify the particular requirements for a chassis configuration conforming to the ANSI/VITA 58.0 base standard.	2013	VITA	27
193	66.2	Optical Interconnect On VPX - ARINC 801 Termini Variant The VITA 66.2 standard defines an ARINC 801 Termini Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2013	VITA	15
194	73.0	VITA 73.0 Rugged Small Form Factor - This document provides mechanical and electrical guidelines for the standardization of switched serial interconnects in small form-factor applications, with specific concern taken to allow deployment in ruggedized envi	2013	VITA	54
195	74.0	Compliant System Small Form Factor Module Base Standard	2013	VITA	67
196	38	Describes a methodology for using IPMI for System Management of VME systems.	2013	VITA	16
197	58.1	Line Replaceable Integrated Electronics Chassis Standard, Liquid Cooled Chassis - The objective of this standard is to identify the particular requirements for a chassis configuration conforming to the ANSI/VITA 58.0 base standard.	2013	VITA	27
198	73.0	VITA 73.0 Rugged Small Form Factor - This document provides mechanical and electrical guidelines for the standardization of switched serial interconnects in small form-factor applications, with specific concern taken to allow deployment in ruggedized envi	2013	VITA	54
199	75.0	VITA 75 Rugged Small Form Factor - This draft standard for a rugged small form factor describes overall subsystem attributes such as the envelope of the subsystem box and the organization of the dot specifications.	2012	VITA	23
200	75.11	This draft standard provides requirements for front panels, connectors, signal pin assignments, and power for VITA 75 subsystems.	2012	VITA	142
201	75.20	Rugged Small Form Factor ù Cooled via Free Air Convection	2012	VITA	26
202	75.22	This draft standard standardizes mounting and cooling for conduction to a cold plate cooled VITA 75 subsystems.	2012	VITA	20
203	66.1	Optical Interconnect On VPX - MT Variant â__The VITA 66.1 standard defines an MT Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2012	VITA	14
204	10	SKYchannel - This standard was withdrawn as an American National Standard in 2012 and is provided for historical reference only. This standard defines a packet switched cross bar interconnect that runs on the VMEbus P2 connector.	2012	VITA	42
205	75.0	VITA 75 Rugged Small Form Factor - This draft standard for a rugged small form factor describes overall subsystem attributes such as the envelope of the subsystem box and the organization of the dot specifications.	2012	VITA	22
206	75.11	This draft standard provides requirements for front panels, connectors, signal pin assignments, and power for VITA 75 subsystems.	2012	VITA	141
207	75.20	Rugged Small Form Factor ù Cooled via Free Air Convection	2012	VITA	25
208	75.22	This draft standard standardizes mounting and cooling for conduction to a cold plate cooled VITA 75 subsystems.	2012	VITA	19
209	12	M-Module - This standard defines a mezzanine module specification for small sized printed circuit boards.	2012	VITA	60
210	65	The OpenVPX System Specification was created to bring versatile system architectural solutions to the VPX market. Based on the extremely flexible VPX family of standards, the OpenVPX standard uses module mechanical, connectors, thermal, communications pro	2012	VITA	555

211	67.1	Coaxial Interconnect on VPX, 3U, 4 Position, SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a 3U VITA 46 interface containing multi-position blind mate analog	2012	VITA	23
212	67.2	Coaxial Interconnect on VPX, 8 Position SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a VITA 46 interface containing multi-position blind mate analog connecto	2012	VITA	24
213	67.0	Coaxial Interconnect on VPX - Base Standard - The objective of this standard is to establish a structure for implementing blind mate analog coaxial interconnects with VPX backplanes and plug-in modules, and to define a specific family of interconnects and	2012	VITA	25
214	66.3	Optical Interconnect On VPX - Mini-Expanded Beam Variant The VITA 66.3 standard defines an MT Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2012	VITA	16
215	60.0	Alternative Connector for VPX - This standard provides an alternate connector to the one specified in the VITA 46.0 VPX Baseline Standard. Because the 46.0 and the 60.0 connectors are not intermateable, a VITA 60.0 module will not plug into a VITA 46.0.0	2012	VITA	45
216	62.0	VPX: Modular Power Supply - This standard provides a set of requirements for power supply modules that can be used in VPX systems.	2012	VITA	91
217	10	SKYchannel - This standard was withdrawn as an American National Standard in 2012 and is provided for historical reference only. This standard defines a packet switched cross bar interconnect that runs on the VMEbus P2 connector.	2012	VITA	44
218	12	M-Module - This standard defines a mezzanine module specification for small sized printed circuit boards.	2012	VITA	62
219	51.0	Reliability Prediction - This document provides an electronics failure rate prediction standard, and establishes a Community of Practice. It addresses the limitations of existing prediction practices with a series of subsidiary specifications that contain	2012	VITA	28
220	46.3	Serial RapidIO on VPX Fabric Connector - This standard assigns Serial RapidIO ports to the VPX P1/J1 connector.	2012	VITA	47
221	46.4	PCI Express_ on the VPX Fabric Connector - The objective of this standard is the implementation of the PCI Express_ Fabric in the VITA46 environment and to define the mapping of the PCI Express Links on the VPX connector.	2012	VITA	21
222	46.7	Ethernet on VPX Fabric Connector - The objectives of this standard are to assign backplane Ethernet links to the VPX P1/J1 connector and to provide rules and recommendations for the use of Ethernet over backplane media.	2012	VITA	27
223	42.2	XMC Serial RapidIO Protocol Layer Standard - This standard defines the implementation of Serial RIO on VITA 42.0, XMC.	2012	VITA	17
224	42.1	XMC Switched Mezzanine Card: Parallel RapidIO 8/16 LP-LVDS Protocol Layer Standard - This standard defines the implementation of Parallel RIO on VITA 42.0, XMC.	2012	VITA	32
225	46.8	InfiniBand on VPX Fabric Connector - The objectives of this draft standard are to assign InfiniBand ports to the VPX connectors and to provide rules and recommendations for the use of the assigned InfiniBand ports.	2011	VITA	52
226	51.2	Physics of Failure Reliability Predictions - This specification provides standard processes, instructions and default parameters for using the Physics of Failure (PoF) approach for modeling the reliability of electronic products. It includes a discussion	2011	VITA	57
227	6	SCSA - This standard defines an isochronous backplane bus for telephony applications on the VMEbus P2 connector.	2011	VITA	55
228	4.1	IP I/O Mapping to VME64x - This standard defines the pin assignments from IP Modules to the VME64x P0 and P2 connectors.	2011	VITA	15
229	4	IP Module - This standard defines the requirements for a business card sized mezzanine module printed circuit board.	2011	VITA	97
230	5.1	RACEway Interlink - This standard defines a high speed circuit switched point to point interconnect for use between VMEbus modules via the P2 connector.	2011	VITA	72
231	6.1	SCSA Extensions - This standard provides feature extensions to the ANSI/VITA 6 standard.	2011	VITA	33
232	1.6	Keying for Conduction Cooled VME64x.	2011	VITA	29
233	1	VME64 Standard - This standard covers the main body of the VMEbus specification. It includes both 32 bit and 64 bit usage.	2011	VITA	305
234	3	Board Level Live Insertion - This standard defines several methodologies for using VMEbus modules in a live insertion framework.	2011	VITA	66

235	1.1	VME64 Extensions - This standard covers extensions to the VME64 specification including the 160 pin connector, geographical addressing, and added power pins.	2011	VITA	100
236	1.3	VME64x 9U x 400 mm Format - This standard defines a 9U x 400 mm board layout for use within the VMEbus framework.	2011	VITA	48
237	35	Provides pin assignments for PMC P4 connector to VME P0 and P2 connectors.	2011	VITA	18
238	30	2mm Connector Practice for Euroboard Systems - This standards provides the dimensions for Euroboard systems that use 2mm connectors.	2011	VITA	37
239	41.2	VXS 4X Serial RapidIO Protocol Layer Standard - This standard describes a method for implementing Serial Rapid I/O on ANSI/VITA 41.0, VXS.	2011	VITA	27
240	20	CCPMC - Conduction Cooled PMC - This standard defines the mechanical requirements for compliance with conduction cooled PMC modules.	2011	VITA	21
241	17	Front Panel Data Port (FPDP) - This standard defines a point to point data interconnect for use on front panel Eurocard modules.	2011	VITA	46
242	23	VME64 Extensions for Physics - This standard defines a series of recommended practices for the use of VMEbus in the physics community.	2011	VITA	123
243	26	Myrinet - This standard defines a packet switched interconnect protocol for implementation in a VMEbus environment.	2011	VITA	52
244	66.0	Optical Interconnect on VPX - Base Standard -- The VITA 66.0 base standard defines physical features of a stand-alone compliant blind mate Optical Interconnect for use in VPX systems.	2011	VITA	19
245	66.1	Optical Interconnect On VPX - MT Variant The VITA 66.1 standard defines an MT Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2011	VITA	14
246	17	Front Panel Data Port (FPDP) - This standard defines a point to point data interconnect for use on front panel Eurocard modules.	2011	VITA	46
247	1.6	Keying for Conduction Cooled VME64x.	2011	VITA	27
248	3	Board Level Live Insertion - This standard defines several methodologies for using VMEbus modules in a live insertion framework.	2011	VITA	64
249	4	IP Module - This standard defines the requirements for a business card sized mezzanine module printed circuit board.	2011	VITA	95
250	4.1	IP I/O Mapping to VME64x - This standard defines the pin assignments from IP Modules to the VME64x P0 and P2 connectors.	2011	VITA	13
251	5.1	RACEway Interlink - This standard defines a high speed circuit switched point to point interconnect for use between VMEbus modules via the P2 connector.	2011	VITA	72
252	6	SCSA - This standard defines an isochronous backplane bus for telephony applications on the VMEbus P2 connector.	2011	VITA	53
253	6.1	SCSA Extensions - This standard provides feature extensions to the ANSI/VITA 6 standard.	2011	VITA	31
254	35	Provides pin assignments for PMC P4 connector to VME P0 and P2 connectors.	2011	VITA	16
255	23	VME64 Extensions for Physics - This standard defines a series of recommended practices for the use of VMEbus in the physics community.	2011	VITA	123
256	26	Myrinet - This standard defines a packet switched interconnect protocol for implementation in a VMEbus environment.	2011	VITA	52
257	30	2mm Connector Practice for Euroboard Systems - This standards provides the dimensions for Euroboard systems that use 2mm connectors.	2011	VITA	35
258	1	VME64 Standard - This standard covers the main body of the VMEbus specification. It includes both 32 bit and 64 bit usage.	2011	VITA	303
259	1.1	VME64 Extensions - This standard covers extensions to the VME64 specification including the 160 pin connector, geographical addressing, and added power pins.	2011	VITA	100
260	1.3	VME64x 9U x 400 mm Format - This standard defines a 9U x 400 mm board layout for use within the VMEbus framework	2011	VITA	48
261	46.8	InfiniBand on VPX Fabric Connector - The objectives of this draft standard are to assign InfiniBand ports to the VPX connectors and to provide rules and recommendations for the use of the assigned InfiniBand ports.	2011	VITA	51

262	65	The OpenVPX System Specification was created to bring versatile system architectural solutions to the VPX market. Based on the extremely flexible VPX family of standards, the OpenVPX standard uses module mechanical, connectors, thermal, communications pro	2010	VITA	555
263	57.1	FPGA Mezzanine Card (FMC) Standard - This standard defines the mechanical format and signal assignments for an FPGA mezzanine card interface.	2010	VITA	82
264	53.0	Standard for Commercial Technology Market Surveillance This standard describes the types of market surveillance data needed by Department of Defense program managers in order to develop and implement technology refresh plans.	2010	VITA	24
265	51.3	Qualification and Environmental Stress Screening in Support of Reliability Predictions - This standard provides rules, permissions, and observations to assure that cost effective Qualification and Environmental Stress Screening support valid reliability p	2010	VITA	21
266	48.0	Mechanical Specification for Microcomputers Using Ruggedized Enhanced Design Implementation (REDI)	2010	VITA	17
267	48.5	Establishes the design requirements for an air-flow-through cooled plug-in unit with a form factor as close to 6U as possible while retaining the VITA 46 connector layout. Unlike ANSI/VITA 48.1, which uses cooling air impinged directly upon the components	2010	VITA	33
268	48.2	This Standard defines the mechanical requirements that are needed to ensure the mechanical interchangeability of conduction cooled 3U and 6U Plug-In Modules and defines the features required to achieve Two Level Maintenance compatibility.	2010	VITA	53
269	48.1	This standard defines the mechanical requirements that are needed to insure the mechanical interchangeability of air cooled 3U and 6U Plug-In Modules and define the features required to achieve Two Level Maintenance compatibility.	2010	VITA	48
270	46.9	PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard - This VITA 46 (VPX) subsidiary standard defines PMC or XMC mezzanine rear I/O pin mappings to VITA 46.0 plug-in module backplane connectors.	2010	VITA	70
271	46.4	PCI Express on the VPX Fabric Connector - The objective of this standard is the implementation of the PCI Express Fabric in the VITA46 environment and to define the mapping of the PCI Express Links on the VPX connector.	2010	VITA	17
272	46.10	Rear Transition Module for VPX	2009	VITA	38
273	42.6	XMC 10 Gigabit Ethernet 4-Lane Protocol Layer Standard - This standard defines a method for supporting 10 Gigabit Ethernet using XAUI switched interconnect protocol on the XMC form factor.	2009	VITA	19
274	49.1	This standard specifies an optional encapsulation protocol for VITA-49.0 (VRT) packets.	2009	VITA	17
275	49.1	This standard specifies an optional encapsulation protocol for VITA-49.0 (VRT) packets.	2009	VITA	18
276	49.0	The VITA Radio Transport (VRT) standard defines a transport-layer protocol designed to promote interoperability between RF (radio frequency) receivers and signal processing equipment in a wide range of applications.	2009	VITA	179
277	49.0	The VITA Radio Transport (VRT) standard defines a transport-layer protocol designed to promote interoperability between RF (radio frequency) receivers and signal processing equipment in a wide range of applications.	2009	VITA	184
278	41.6	VXS 1X Gbit Ethernet - This standard describes a method for implementing Ethernet as a control channel on ANSI/VITA 41.0, VXS.	2009	VITA	35
279	41.6	VXS 1X Gigabit Ethernet Control Channel Layer Standard	2009	VITA	32
280	31.1	Gigabit Ethernet on VME64x Backplanes - This standard defines a pin assignment and interconnection methodology for implementing a 10/100/1000BASE-T Ethernet switched network on a ANSI/VITA 1.1 VME64x backplane.	2009	VITA	18
281	17.1	Serial Front Panel Data Port (sFPDP) - This standard defines Serial FPDP, a high-speed low-latency serial communications protocol for use in high-speed data transfer applications, typically using a fiber optic link.	2009	VITA	43
282	58.0	This standard provides common design and performance requirements for a family of integrated electronic chassis incorporating updated industry standard high speed electronic assemblies and designed for rugged environments.	2009	VITA	27
283	57.1	FPGA Mezzanine Card (FMC) Standard - This standard defines the mechanical format and signal assignments for an FPGA mezzanine card interface.	2008	VITA	79
284	30.1	2mm Connector Practice for Conduction Cooled Euroboard Systems - This standard defines the dimensions for conduction cooled Euroboards when used with 2mm connectors.	2008	VITA	37
285	42.0	XMC	2008	VITA	40
286	46.7	Ethernet on VPX Fabric Connector - The objectives of this standard are to assign backplane Ethernet links to the VPX P1/J1 connector and to provide rules and recommendations for the use of Ethernet over backplane media.	2008	VITA	21

287	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2007	VITA	109
288	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2007	VITA	107
289	47	This standard defines environmental, design and construction, safety, and quality requirements for commercial-off-the-shelf (COTS) plug-in units (cards, modules, etc.) intended for mobile applications.	2007	VITA	22
290	41.1	VXS 4X InfiniBand Protocol Layer Standard - This standard describes a method for using the InfiniBand protocol on ANSI/VITA 41.0, VXS.	2006	VITA	26
291	41.0	VXS VMEbus Switched Serial Standard - This standard defines a method for using switched serial fabrics within the VMEbus framework.	2006	VITA	60
292	13	VMEbus Pin Assignment Standard for ISO/IEC 14575 (IEEE Std. 1355-1995 (H.I.C.)) - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only.	2006	VITA	14
293	19.1	BusNet Media Access Control - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines the media access control layer for the BusNet backplane software protocol.	2006	VITA	64
294	19.2	BusNet Link Layer Control - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines the link layer control layer for the Busnet backplane software protocol.	2006	VITA	18
295	25	VISION - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines a software application interface for VMEbus modules.	2006	VITA	135
296	29	PC.MIP - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines the mechanical form factor and the pin assignments for a small form factor mezzanine module based on the PCI bus.	2006	VITA	66
297	40	Service and Status Indicator Standard. This standard defines the colors, behaviors, placement, and labeling of service indicator lamps for boards, field replaceable units, and enclosures.	2003	VITA	40
298	17.1	Serial Front Panel Data Port (sFPDP) - This standard defines Serial FPDP, a high-speed low-latency serial communications protocol for use in high-speed data transfer applications, typically using a fiber optic link.	2003	VITA	42
299	1.3	VME64x 9U x 400 mm Format - This standard defines a 9U x 400 mm board layout for use within the VMEbus framework.	2003	VITA	48
300	1.1	VME64 Extensions - This standard covers extensions to the VME64 specification including the 160 pin connector, geographical addressing, and added power pins.	2003	VITA	100
301	40	Service and Status Indicator Standard. This standard defines the colors, behaviors, placement, and labeling of service indicator lamps for boards, field replaceable units, and enclosures.	2002	VITA	37
302	29	PC.MIP - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines the mechanical form factor and the pin assignments for a small form factor mezzanine module based on the PCI bus.	2001	VITA	68
303	1.5	2eSST - This standard defines a new VME protocol that allows data transfers of up to 320 Mbytes/second. Reaffirmed in 2009. Stabilized in 2014.	1999	VITA	51
304	5.1	RACEway Interlink - This standard defines a high speed circuit switched point to point interconnect for use between VMEbus modules via the P2 connector.	1999	VITA	74
305	1.4	VME64x Live Insertion System Requirements	1998	VITA	29
306	26	Myrinet - This standard defines a packet switched interconnect protocol for implementation in a VMEbus environment.	1998	VITA	54
307	23	VME64 Extensions for Physics - This standard defines a series of recommended practices for the use of VMEbus in the physics community.	1998	VITA	125
308	17	Front Panel Data Port (FPDP) - This standard defines a point to point data interconnect for use on front panel Eurocard modules.	1998	VITA	48
309	19.1	BusNet Media Access Control - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines the media access control layer for the BusNet backplane software protocol.	1998	VITA	66
310	19.2	BusNet Link Layer Control - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines the link layer control layer for the Busnet backplane software protocol.	1998	VITA	20
311	19.0	Summary and Introduction to the BusNet Standard	1997	VITA	19

312	25	VISION - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines a software application interface for VMEbus modules.	1997	VITA	137
313	1.1	VME64 Extensions - This standard covers extensions to the VME64 specification including the 160 pin connector, geographical addressing, and added power pins.	1997	VITA	98
314	1.3	VME64x 9U x 400 mm Format - This standard defines a 9U x 400 mm board layout for use within the VMEbus framework	1997	VITA	50
315	4.1	IP I/O Mapping to VME64x - This standard defines the pin assignments from IP Modules to the VME64x P0 and P2 connectors.	1996	VITA	15
316	6.1	SCSA Extensions - This standard provides feature extensions to the ANSI/VITA 6 standard.	1996	VITA	39
317	12	M-Module - This standard defines a mezzanine module specification for small sized printed circuit boards.	1996	VITA	63
318	10	SKYchannel - This standard was withdrawn as an American National Standard in 2012 and is provided for historical reference only. This standard defines a packet switched cross bar interconnect that runs on the VMEbus P2 connector.	1995	VITA	43
319	13	VMEbus Pin Assignment Standard for ISO/IEC 14575 (IEEE Std. 1355-1995 (H.I.C.)) - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only.	1995	VITA	16
320	4	IP Module - This standard defines the requirements for a business card sized mezzanine module printed circuit board.	1995	VITA	97
321	3	Board Level Live Insertion - This standard defines several methodologies for using VMEbus modules in a live insertion framework.	1995	VITA	66
322	1	VME64 Standard - This standard covers the main body of the VMEbus specification. It includes both 32 bit and 64 bit usage.	1994	VITA	305
323	6	SCSA - This standard defines an isochronous backplane bus for telephony applications on the VMEbus P2 connector.	1994	VITA	55